AGLNA014221

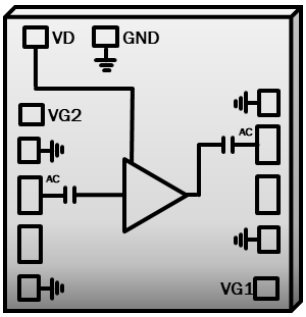
GaAs MMIC
2-20GHz Distributed Amplifier

Typical Applications

- Test Instrumentation
- EW Systems
- Telecom Infrastructure
- EW/ECM Comm Systems

Features

- Frequency Range: 2 – 20 GHz
- Gain: 16dB
- P1dB: + 15dBm
- Self-Biased: VD=+10V @ 50mA Single Supply
- 50Ω Matched DC blocked Input/Output



Electrical Specifications (TA = +25°C, VD = +10V, IDQ = 50mA)

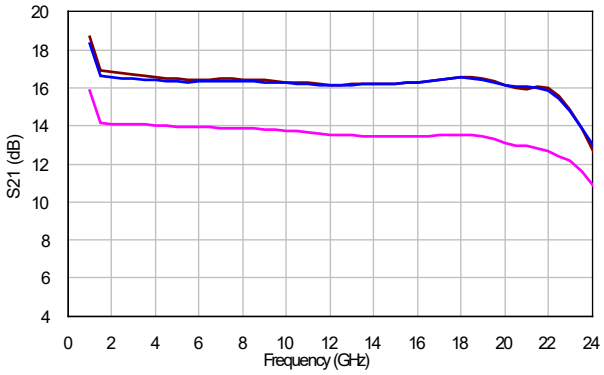
Parameter	Units	Minimum	Typical	Maximum
Frequency	GHz	2		20.0
Gain	dB		16.0	
Gain Flatness	dB		± 0.4	
Noise Figure	dB		2	4
Input Return Loss	dB	10	15	
Output Return Loss	dB	10	12	
P1dB	dBm		15	
Psat	dBm		20	
Supply Voltage	V		+10	
Supply Current	mA		50	
DC Dissipated Power	mW		500	
Package Type			Die	

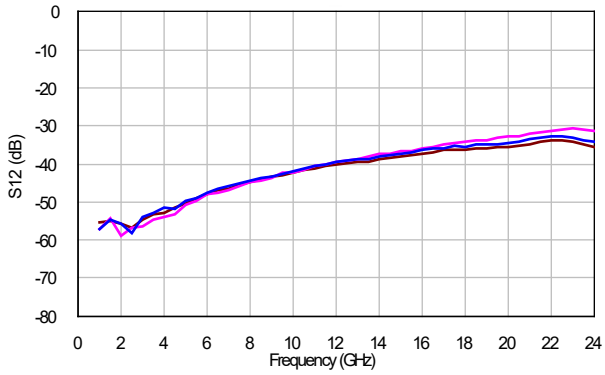
Broadband Amplifiers - Die

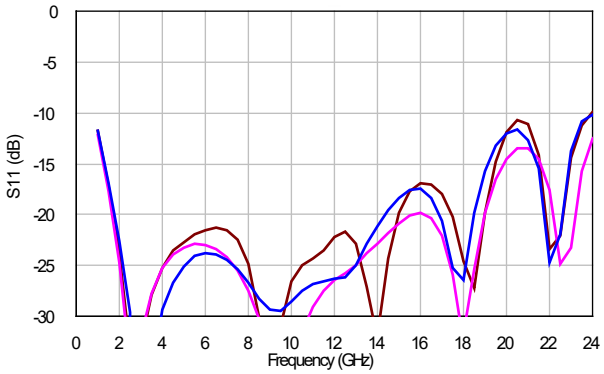
Performance Graphs

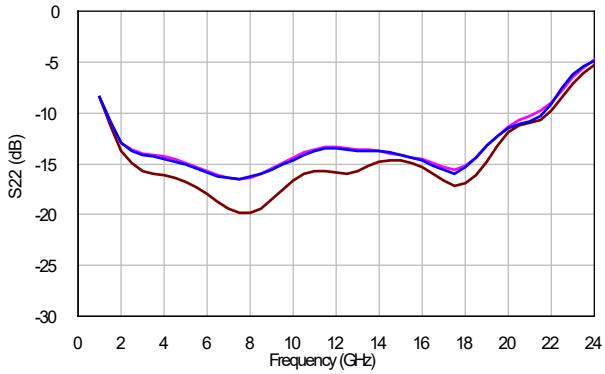
S-Parameters and Noise Figure vs. VD (25°C)

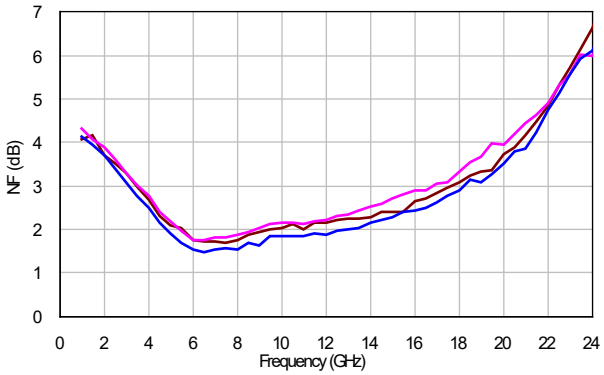
VD=10V (single supply) VD=8V (single supply) VD=10V & IDQ=50mA (Vg=+0.4V)



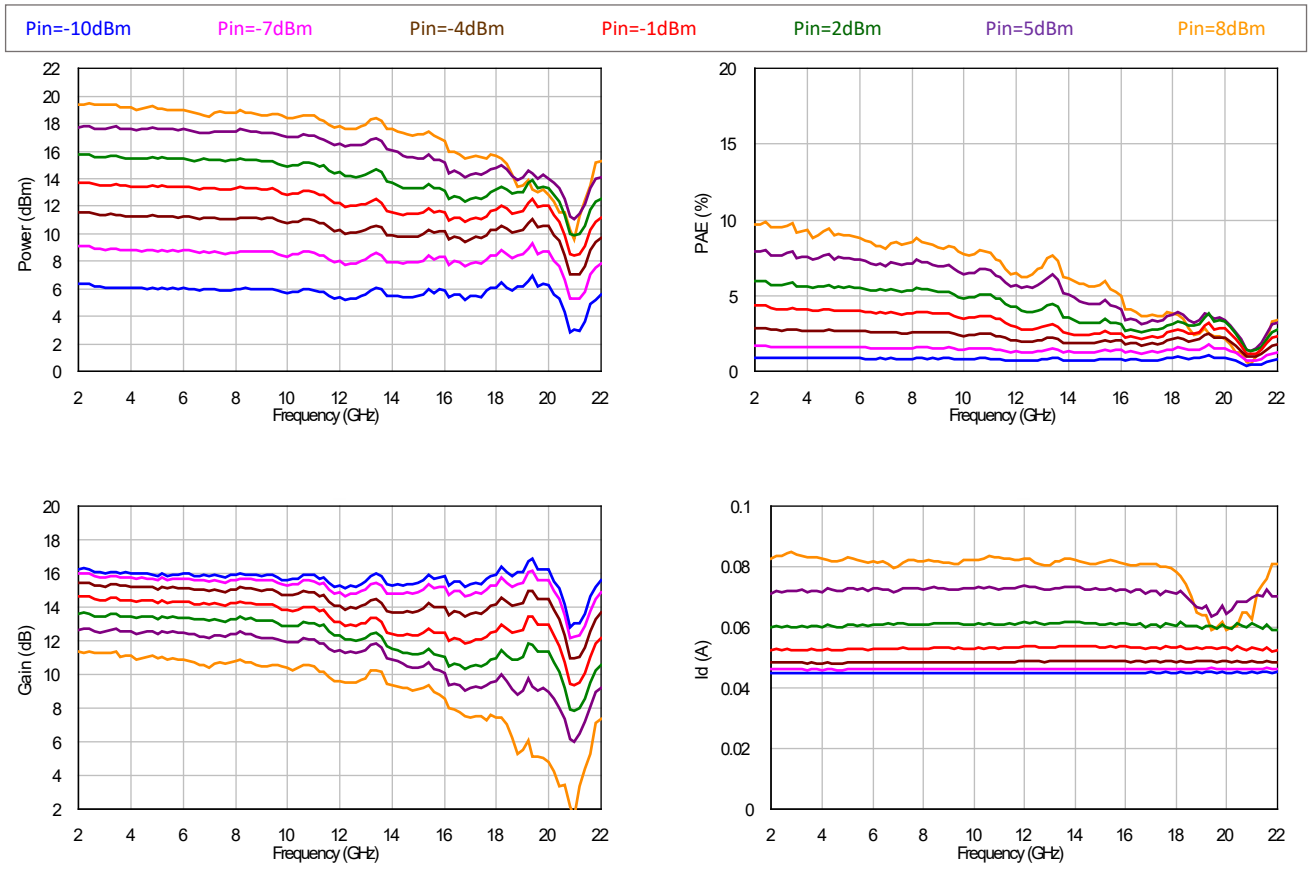




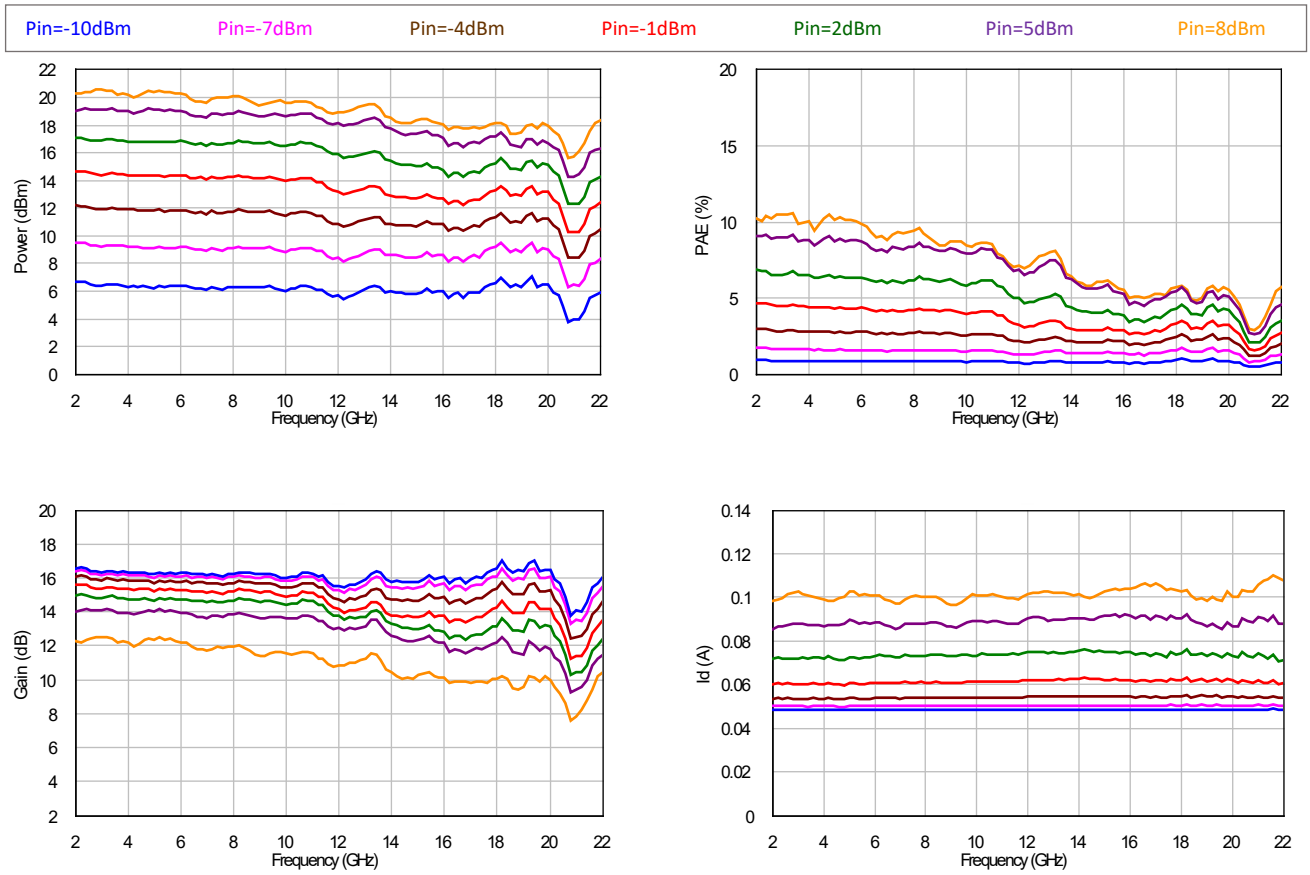




Frequency Response vs. Input Power (25°C, VD=10V, Single-Supply)

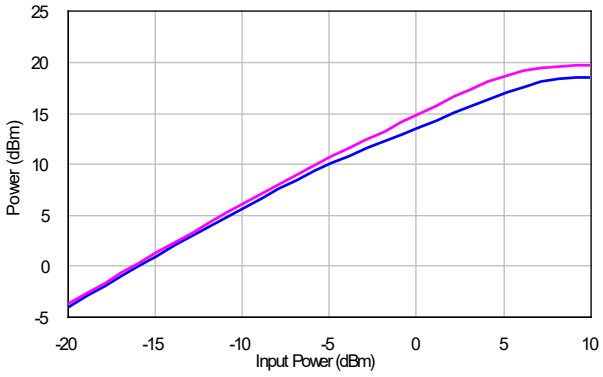


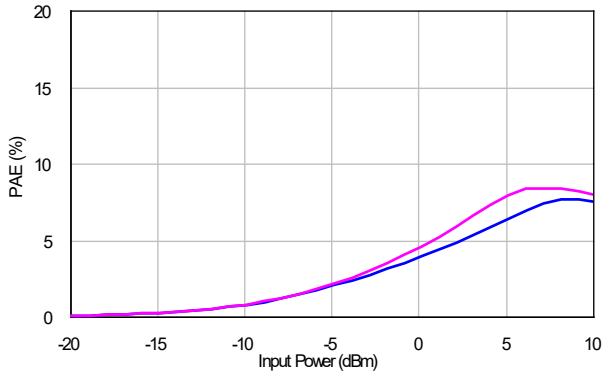
Frequency Response vs. Input Power (25°C, VD=10V & IDQ=50mA, & VG=0.4V)

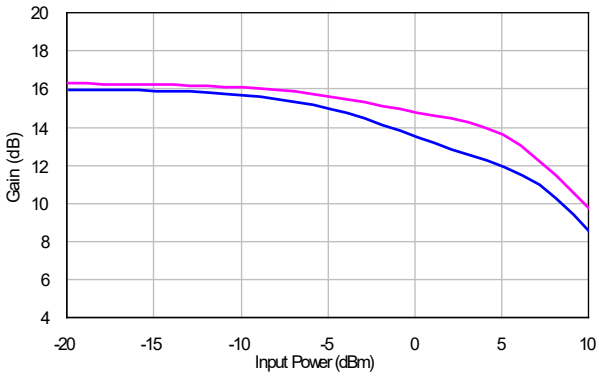


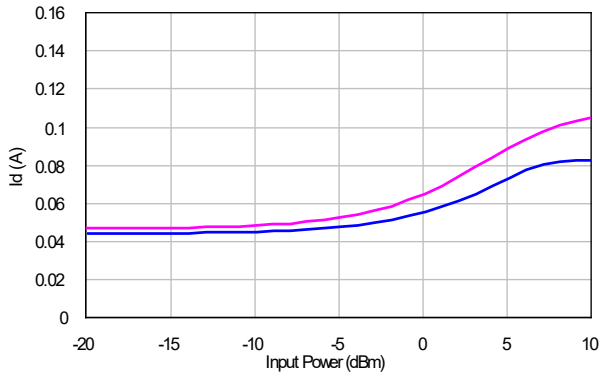
Power Sweep vs. Bias (25°C, 10GHz)

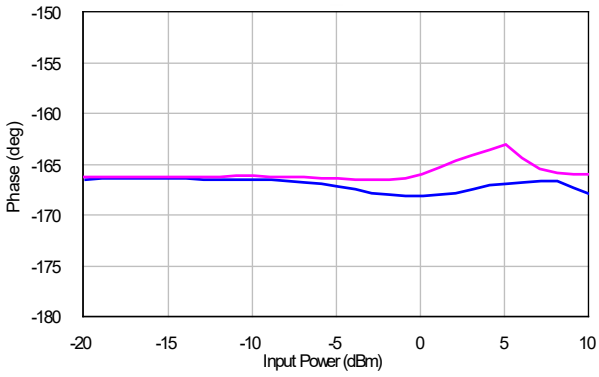
VD=10 (Single Supply) VD=10V & IDQ=50mA (VG=+0.4V)

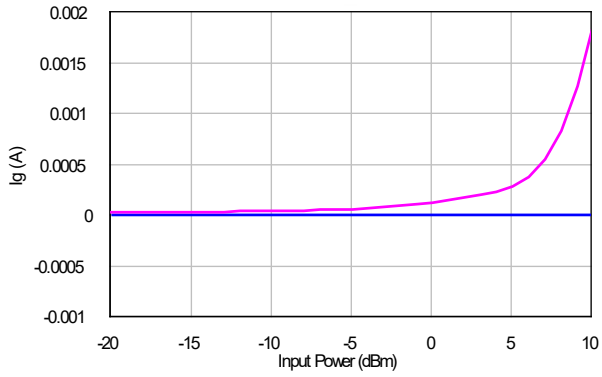












Die Outline Drawing

Die Pad Descriptions

Pad	Function	Pad Size	Description
1	RFIN	100x114µm	DC Blocked 50Ω Matched
2	RFOUT	100x114µm	DC Blocked 50Ω Matched
3	VD	100x100µm	Drain Power Supply, bypass capacitors needed*
4	VG1	100x100µm	No connect, Optional Gate Power Supply for Bias Override*
5	VG2	100x100µm	No connect
Die Bottom	GND	Backside	Epoxy/Solder to Baseplate

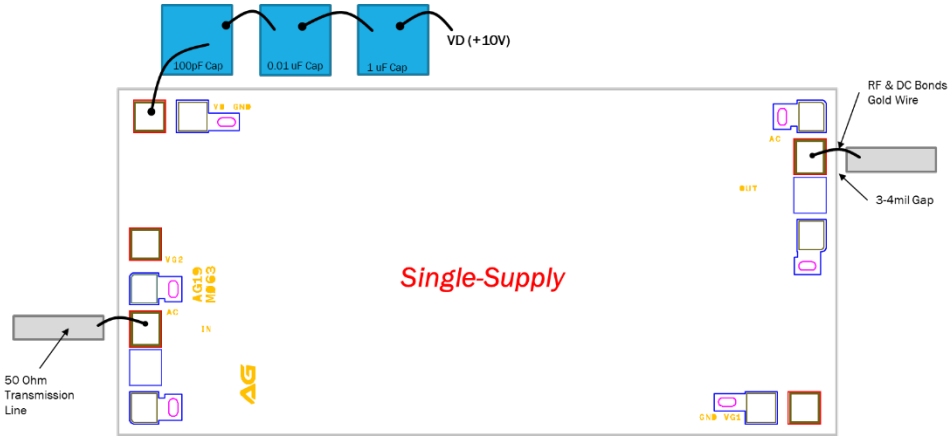
*See Assembly Diagram

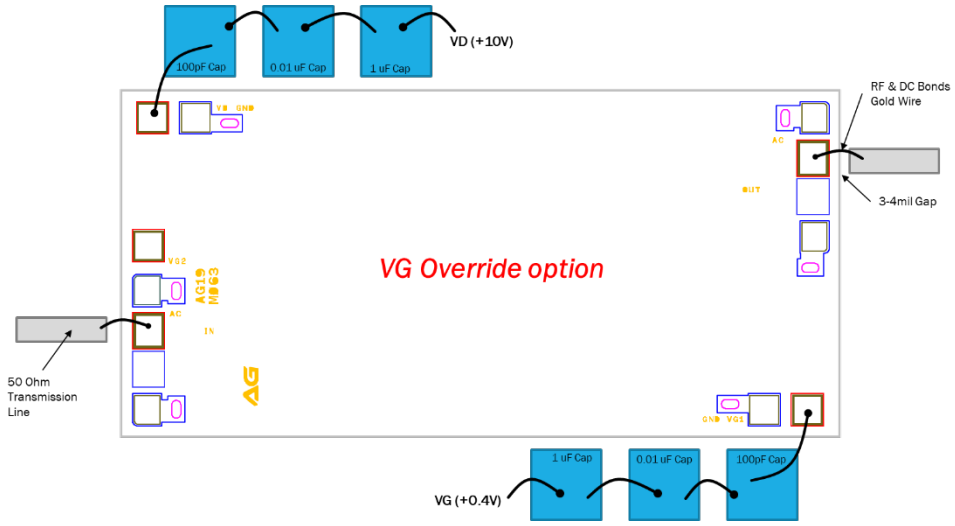
Absolute Maximum Ratings

Parameter	Rating
Drain Bias Voltage (VDD)	+12V DC
RF Input Power (RFIN)	+20dBm*
Channel Temperature	150°C
Storage Temperature	-65 to 150°C
Operating Temperature	-55 to 85°C

*To be tested

Die Assembly Diagrams





Die Assembly Notes:

1. Die Thickness is 100µm
2. Backside and Bondpad metallization: 3µm gold
3. Silver Epoxy or AuSn Eutectic attach MMIC
4. Gap between MMIC and 50 Ohm lines should be 3-4mils
5. Off-Chip bypass capacitor values are approximate

Biasing and Operation

The amplifier has both a single supply biasing mode as well as used in a mode where the current can be adjusted by applying a Vg override voltage to optimize performance. For overriding the bias current use the following biasing procedure:

Turn ON procedure:

1. Set VG to 0.0V.
2. Set VD to Vdq.
3. Adjust VG more positive until Id = Idq.
4. Apply RF signal.

Turn OFF procedure:

1. Turn off RF signal.
2. Reduce VG to 0.0V. Id should be 0mA.
3. Turn off VD.
4. Turn off VG.

Important Notice

The information contained in this Data Sheet and any associated documents is believed to be reliable; however, AmpliTech makes no warranties regarding the Data Sheet Information and assumes no responsibility of liability whatsoever for the use of the said information. All Data Sheet information is subject to change without notice.