Description

The 8TR1111 is optimized for battery operation with enhanced efficiency, operating over a wide voltage supply range from 2.7V to 3.6V, suited for a wide range of applications including battery powered wireless systems.

The 8TR1111 combines a power amplifier (PA), bypass, and a directional TX power Detector. The device also comes integrated with filter networks, and input matching circuitry. Output matching is external. This device is ideal for Sigfox operation at 24dBm.

Table 1: 8TR1111 Wafer Information

Item	Description
Wafer Diameter	200mm
Technology	180nm CMOS

Table 2: 8TR1111 DIE Information

Item	Description
DIE ID	C51011
DIE Size	1650um X 1150um
Pads Size	70um X 70um, 78um X 78um, 137um X 70um, 206um X 70um
Pads Opening	66um X 66um, 74um X 74um, 133um X 66um, 202um X 66um
Wafer Map	Electronic Text File
Manufacturing Facility	HHGrace
Wafer Thickness Maximum	725um
Back Grind Options	Contact BeRex
Back Plane Connection	NA
Backside preparation / metallization	NA
Passivation Material	TEOS+SIN
Passivation Thickness	TEOS-6K+SIN-6K
Bond Pad Material	Al
Bond Pad Thickness	4um
Good Die per Wafer	Contact BeRex
Active Circuits Underneath the Bond Pad	No

Table 3: 8TR1111 Control Logic

"1" = Logic High, "0" = Logic Low

PAEN	Operational Mode
0	Bypass Mode*
1	TX PA Mode

*The Bypass Mode feature provides an ultra-low current consumption, as in a conventional sleep Mode.

Table 4: Ordering Information

Part Nunber	Description
8TR1111	Sub GHz Front-End RFIC in 3mm x 3mm x 0.45mm 16-Pin QFN
8TR1111-EVB	Fully Tested and Characterize Evaluation Board
8TR1111-DWF	Sub GHz Front-End RFIC Die in Wafer Form

Die Pad Layout

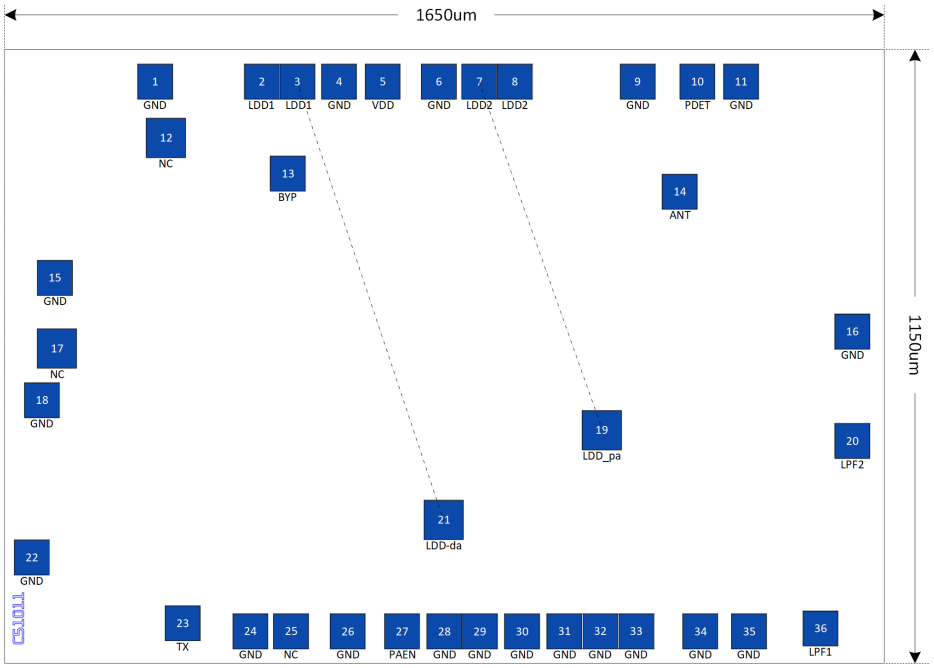

Figure 3 :Die Pad Layout

Table 5: 8TR1111 DIE Pad Coordinates [1]

Pin	Name	Description	X(um)	Y(um)	Pin	Name	Description	X(um)	Y(um)
1	GND	Ground	-542.5	515.0	19	LDD_pa	Connect to LDD2(Pad 7)	295.1	-138.1
2	LDD1	VDD	-342.3	515.0	20	LPF2	Matching Network, node2 [3]	765.0	-158.2
3	LDD1	VDD	-275.8	515.0	21	LDD_da	Connect to LDD1(Pad 3)	-1.3	-306.2
4	GND	Ground	-197.7	515.0	22	GND	Ground	-774.0	-376.5
5	VDD	VDD	-115.8	515.0	23	TX	TX PA Input	-490.8	-499.9
6	GND	Ground	-10.5	515.0	24	GND	Ground	-363.8	-515.0
7	LDD2	VDD [2]	65.8	515.0	25	NC	Not connect	-287.7	-515.0
8	LDD2	VDD [2]	132.3	515.0	26	GND	Ground	-181.5	-515.0
9	GND	Ground	362.5	515.0	27	PAEN	Control Logic pin	-79.5	-515.0
10	PDET	Detector Voltage Output	474.4	515.0	28	GND	Ground	0.1	-515.0
11	GND	Ground	556.4	515.0	29	GND	Ground	66.6	-515.0
12	NC	Not connect	-522.4	409.5	30	GND	Ground	145.6	-515.0
13	BYP	Bypass Port	-293.8	342.5	31	GND	Ground	225.3	-515.0
14	ANT	Antenna port	441.1	308.8	32	GND	Ground	292.6	-515.0
15	GND	Ground	-730.4	147.2	33	GND	Ground	359.9	-515.0
16	GND	Ground	765.0	46.7	34	GND	Ground	479.8	-515.0
17	NC	Not connect	-726.9	14.9	35	GND	Ground	571.2	-515.0
18	GND	Ground	-755.0	-82.0	36	LPF1	Matching Network, node2 [4]	705.2	-509.4

Note1: All pad coordinates refer to the center of the pad relative to the center of the DIE.

Note2: It is recommended to connect to VDD through inductor 2.4nH.

Note3: It is connected to ANT through Switch.

Note4: TX PA Output Port.

Wafer Map

- Scribe line width: 60 um
- Chip Size(1X): X = 1650.000um Y = 1150.000um
- Shot Array: X = 9 Y = 7
- Shot Size: X = 23880.000 Y = 31400.000
- Total Chip Numbers: 13906
- Shot shift: X = 0 Y = -11284
- Wafer Edge: 3200um
- Notch in the bottom
- Alignment mark is shrink Version

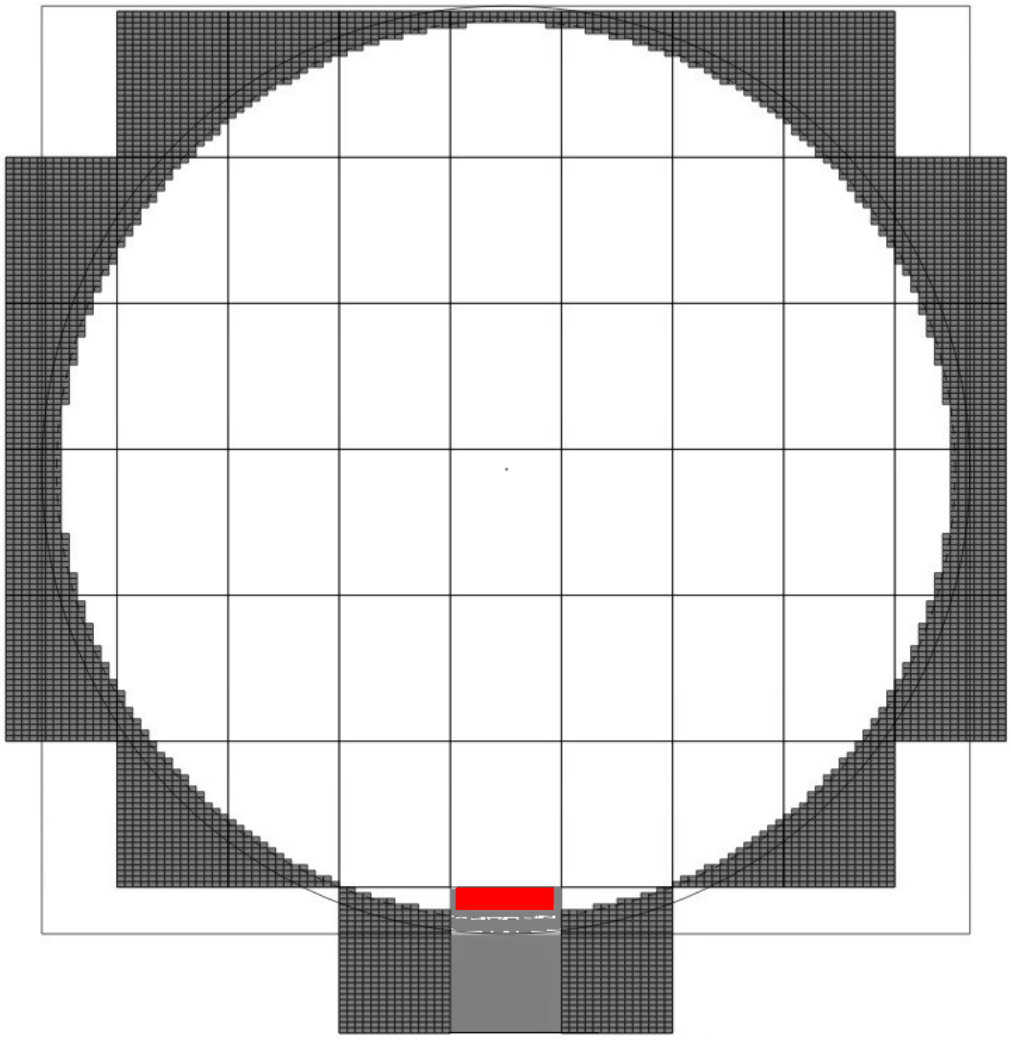

Figure 8: 8TR1111 Wafer Map

Table 6: 8TR1111 Absolute Maximum Ratings

Parameter	Units	Minimum	Maximum
Supply Voltage (VDD)	V	0	3.7
Control Logic Pin (PAEN)	V	0	VDD
Transmit Output Power at ANT Port	dBm		26
Transmit Input Power at TX Port	dBm		10
Bypass Mode Power at ANT or BYP Port	dBm		20
Storage Temperature	°C	-40	150

Note: Sustained operation at or above the Absolute Maximum Ratings for any single or combinations of the above parameters may result in permanent damage to the device and is not recommended. All Maximum RF Input Power Ratings assume 50Ω terminal impedance.

Table 7: 8TR1111 Recommended Operating Conditions

Parameter	Units	Minimum	Typical	Maximum
Supply Voltage (VDD, recommended)	V	2.7	3.3	3.6
Supply Voltage (VDD, extend supply voltage)**	V	1.8		3.6
Control Pin - Logic High State	V	1.2		VDD*
Control Pin - Logic Low State	V	0		0.4
Control Pin Current (Logic High, 1.8V)	uA		0.2	
Operating Frequency Range	GHz	0.85		0.93
Operating Temperature	°C	-40	25	125

*For Control Voltages > 3.0V, a 10kΩ series resistor should be used at the Control Logic Pins.
**Functional working with degraded performance for the supply voltage range 1.8V to 2.7V.

ESD Handling Information

Electro Static Discharge (ESD) can cause immediate (or latent) failures in semiconductor Integrated Circuits (ICs). BeRex, Inc. RFIC products are designed with integral ESD protection structures, and all IC products are tested to meet industry standards for ESD event survival. Users must adhere to all precautions for handling ESD sensitive devices throughout the manufacturing, test, shipping, handling, or operational processes, and during field service operations in order to achieve optimum system performance and life expectancy.
Electrostatic Discharge Rating - HBM: TBD