ICM-20601 Datasheet

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1. GENERAL DESCRIPTION

1.2 PURPOSE AND SCOPE

This document is a product specification, providing a description, specifications, and design related information on the ICM-20601™ MotionTracking device. The device is housed in a small 3x3x0.75mm 16-pin LGA package.

1.3 PRODUCT OVERVIEW

The ICM-20601 is a 6-axis MotionTracking device that combines a 3-axis gyroscope, and a 3-axis accelerometer in a small 3x3x0.75mm (16-pin LGA) package. It also features a 512-byte FIFO that can lower the traffic on the serial bus interface, and reduce power consumption by allowing the system processor to burst read sensor data and then go into a low-power mode. ICM-20601, with its 6-axis integration, enables manufacturers to eliminate the costly and complex selection, qualification, and system level integration of discrete devices, guaranteeing optimal motion performance for consumers.

The gyroscope has a programmable full-scale range up to ±4000 degrees/sec. The accelerometer has a user-programmable accelerometer full-scale range up to ±32*g*. Factory-calibrated initial sensitivity of both sensors reduces production-line calibration requirements.

Other industry-leading features include on-chip 16-bit ADCs, programmable digital filters, an embedded temperature sensor, and programmable interrupts. The device features I^2C and SPI serial interfaces, a VDD operating range of 1.71 to 3.45V, and a separate digital IO supply, VDDIO from 1.71V to 3.45V. Communication with all registers of the device is performed using either I^2C at 400kHz or SPI at 8MHz.

By leveraging its patented and volume-proven CMOS-MEMS fabrication platform, which integrates MEMS wafers with companion CMOS electronics through wafer-level bonding, InvenSense has driven the package size down to a footprint and thickness of 3x3x0.75mm (16-pin LGA), to provide a very small yet high performance low cost package. The device provides high robustness by supporting 10,000*g* shock reliability.

1.4 APPLICATIONS

- High Impact Sports
- Wearable Sensors

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2. FEATURES

2.1 GYROSCOPE FEATURES

The triple-axis MEMS gyroscope in the ICM-20601 includes a wide range of features:

- Digital-output X-, Y-, and Z-axis angular rate sensors (gyroscopes) with a user-programmable full-scale range of ±500, ±1000, ±2000, and ±4000°/sec and integrated 16-bit ADCs
- Digitally-programmable low-pass filter
- Factory calibrated sensitivity scale factor
- Self-test

2.2 ACCELEROMETER FEATURES

The triple-axis MEMS accelerometer in ICM-20601 includes a wide range of features:

- Digital-output X-, Y-, and Z-axis accelerometer with a programmable full scale range of ±4*g*, ±8*g*, ±16*g* and ±32*g* and integrated 16-bit ADCs
- User-programmable interrupts
- Wake-on-motion interrupt for low power operation of applications processor
- Self-test

2.3 ADDITIONAL FEATURES

The ICM-20601 includes the following additional features:

- Smallest and thinnest LGA package for portable devices: 3x3x0.75mm (16-pin LGA)
- Minimal cross-axis sensitivity between the accelerometer and gyroscope axes
- 512 byte FIFO buffer enables the applications processor to read the data in bursts
- Digital-output temperature sensor
- User-programmable digital filters for gyroscope, accelerometer, and temp sensor
- 10,000 *g* shock tolerant
- 400kHz Fast Mode I^2C for communicating with all registers
- 8MHz SPI serial interface for communicating with all registers
- MEMS structure hermetically sealed and bonded at wafer level
- RoHS and Green compliant

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3. ELECTRICAL CHARACTERISTICS

3.1 GYROSCOPE SPECIFICATIONS

Typical Operating Circuit of section 0, VDD = 1.8 V, VDDIO = 1.8 V, T_A = 25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
GYROSCOPE SENSITIVITY						
Full-Scale Range	FS_SEL=0		±500		°/s	3
	FS_SEL=1		±1000		°/s	3
	FS_SEL=2		±2000		°/s	3
	FS_SEL=3		±4000		°/s	3
Gyroscope ADC Word Length			16		bits	3
Sensitivity Scale Factor	FS_SEL=0		65.5		LSB/(°/s)	3
	FS_SEL=1		32.8		LSB/(°/s)	3
	FS_SEL=2		16.4		LSB/(°/s)	3
	FS_SEL=3		8.2		LSB/(°/s)	3
Sensitivity Scale Factor Tolerance	25°C		±2		%	2
Sensitivity Scale Factor Variation Over Temperature	-40°C to +85°C		±3		%	1
Nonlinearity	Best fit straight line; 25°C		±0.3		%	1
Cross-Axis Sensitivity			±2		%	1
ZERO-RATE OUTPUT (ZRO)						
Initial ZRO Tolerance	25°C		±5		°/s	2
ZRO Variation Over Temperature	-40°C to +85°C		±0.1		°/s/°C	1
GYROSCOPE NOISE PERFORMANCE (FS_SEL=0)						
Noise Spectral Density			0.013		°/s/√Hz	1
Gyroscope Mechanical Frequencies		25	27	29	KHz	2
Low Pass Filter Response	Programmable Range	5		250	Hz	3
Gyroscope Start-Up Time	From Sleep mode		35		ms	1
Output Data Rate	Standard (duty-cycled) mode	3.91		500	Hz	1
	Low-Noise (active) mode	4		8000	Hz	1

Table 1. Gyroscope Specifications

Notes:

1. Derived from validation or characterization of parts, not guaranteed in production.
2. Tested in production.
3. Guaranteed by design.

3.2 ACCELEROMETER SPECIFICATIONS

Typical Operating Circuit of section 0, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS	NOTES
ACCELEROMETER SENSITIVITY							
Full-Scale Range	AFS_SEL=0			±4		*g*	3
	AFS_SEL=1			±8		*g*	3
	AFS_SEL=2			±16		*g*	3
	AFS_SEL=3			±32		*g*	3
ADC Word Length	Output in two's complement format			16		bits	3
Sensitivity Scale Factor	AFS_SEL=0			8,192		LSB/*g*	3
	AFS_SEL=1			4,096		LSB/*g*	3
	AFS_SEL=2			2,048		LSB/*g*	3
	AFS_SEL=3			1,024		LSB/*g*	3
Initial Tolerance	Component-level			±2		%	2
Sensitivity Change vs. Temperature	-40°C to +85°C AFS_SEL=0 Component-level			±0.016		%/°C	1
Nonlinearity	Best Fit Straight Line			±0.5		%	1
Cross-Axis Sensitivity				±2		%	1
ZERO-G OUTPUT							
Initial Tolerance	Component-level, all axes			±60		m*g*	1
Zero-G Level Change vs. Temperature	-40°C to +85°C, Board-level	X and Y axes		±0.5		mg/°C	1
		Z axis		±1		mg/°C	1
NOISE PERFORMANCE							
Noise Spectral Density				390		µg/√Hz	1
Low Pass Filter Response	Programmable Range		5		218	Hz	3
Intelligence Function Increment				4		mg/LSB	3
Accelerometer Startup Time	From Sleep mode			20		ms	1
	From Cold Start, 1ms V_{DD} ramp			30		ms	1
Output Data Rate	Standard (duty-cycled) mode		0.24		500	Hz	1
	Low-Noise (active) mode		4		4000	Hz	

Table 2. Accelerometer Specifications

Notes:

1. Derived from validation or characterization of parts, not guaranteed in production.
2. Tested in production.
3. Guaranteed by design.

3.3 ELECTRICAL SPECIFICATIONS

3.3.1 D.C. Electrical Characteristics

Typical Operating Circuit of section 0, VDD = 1.8 V, VDDIO = 1.8 V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SUPPLY VOLTAGES						
VDD		1.71	1.8	3.45	V	1
VDDIO		1.71	1.8	3.45	V	1
SUPPLY CURRENTS						
Low-Noise Mode	6-axis Gyroscope + Accelerometer		3		mA	1
	3-axis Gyroscope		2.6		mA	1
	3-axis Accelerometer, 4kHz ODR		390		µA	1
Accelerometer Standard Mode	100Hz ODR, 1x averaging		57		µA	1
Gyroscope Standard Mode	100Hz ODR, 1x averaging		1.6		mA	1
Gyroscope Standard Mode	10Hz ODR, 1x averaging		1.3		mA	1
6-Axis Standard Mode (Gyroscope Standard Mode; Accelerometer Low-Noise Mode)	100Hz ODR, 1x averaging		1.9		mA	1
Full-Chip Sleep Mode			6		µA	1
TEMPERATURE RANGE						
Specified Temperature Range	Performance parameters are not applicable beyond Specified Temperature Range	-40		+85	°C	1

Table 3. D.C. Electrical Characteristics

Notes:

1. Derived from validation or characterization of parts, not guaranteed in production.

3.3.2 Standard (Duty-Cycle) Mode Noise and Power Performance:

The following tables contain Gyroscope and Accelerometer noise and current consumption values for standard (duty-cycle) mode, for various ODRs and averaging filter settings. Please refer to the ICM-20601 Register Map for further information about the registers referenced in the tables below.

FCHOICE_B		0	0	0	0	0	0	0	0
G_AVGCFG		0	1	2	3	4	5	6	7
Averages		1x	2x	4x	8x	16x	32x	64x	128x
Ton (ms)		1.73	2.23	3.23	5.23	9.23	17.23	33.23	65.23
Noise BW (Hz)		650.8	407.1	224.2	117.4	60.2	30.6	15.6	8.0
Noise (dps) TYP based on 0.013º/s/√Hz		0.33	0.26	0.19	0.14	0.10	0.07	0.05	0.04
SMPLRT_DIV	ODR (Hz)	Current Consumption (mA) TYP							
255	3.9	1.3	1.3	1.3	1.3	1.4	1.4	1.5	1.8
99	10.0	1.3	1.3	1.4	1.4	1.5	1.6	1.9	2.5
64	15.4	1.4	1.4	1.4	1.5	1.6	1.8	2.2	N/A
32	30.3	1.4	1.4	1.5	1.6	1.8	2.2	N/A	
19	50.0	1.5	1.5	1.6	1.8	2.1	2.8		
9	100.0	1.6	1.7	1.9	2.2	3.0	N/A		
7	125.0	1.7	1.8	2.0	2.5	N/A			
4	200.0	1.9	2.1	2.5	N/A				
3	250.0	2.1	2.3	2.7					
2	333.3	2.3	2.6	N/A					
1	500.0	2.9	N/A						

Table 4. Gyroscope Noise and Current Consumption

ACCEL_FCHOICE_B		1	0	0	0	0
A_DLPF_CFG		x	7	7	7	7
DEC2_CFG		x	0	1	2	3
Averages		1x	4x	8x	16x	32x
Ton (ms)		1.084	1.84	2.84	4.84	8.84
Noise BW (Hz)		1100.0	441.6	235.4	121.3	61.5
Noise (mg) TYP based on 390µg/√Hz		12.9	8.2	6.0	4.3	3.1
SMPLRT_DIV	ODR (Hz)	Current Consumption (µA) TYP				
255	3.9	8.4	9.4	10.8	13.6	19.2
127	7.8	9.8	11.9	14.7	20.3	31.4
63	15.6	12.8	17.0	22.5	33.7	55.9
31	31.3	18.7	27.1	38.2	60.4	104.9
15	62.5	30.4	47.2	69.4	113.9	202.8
7	125.0	57.4	87.5	132.0	220.9	N/A
3	250.0	100.9	168.1	257.0	N/A	
1	500.0	194.9	329.3	N/A		

Table 5. Accelerometer Noise and Current Consumption

3.3.3 A.C. Electrical Characteristics

Typical Operating Circuit of section 0, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SUPPLIES						
Supply Ramp Time (T_{RAMP})	Monotonic ramp. Ramp rate is 10% to 90% of the final value	0.01		100	ms	1
TEMPERATURE SENSOR						
Operating Range	Ambient	-40		85	°C	1
Room Temperature Offset	25°C		0		°C	1
Sensitivity	Untrimmed		326.8		LSB/°C	1
POWER-ON RESET						
Supply Ramp Time (T_{RAMP})	Valid power-on RESET	0.01		100	ms	1
Start-up time for register read/write	From power-up		11	100	ms	1
	From sleep			5	ms	1
I^2C ADDRESS	AD0 = 0 AD0 = 1		1101000 1101001			
DIGITAL INPUTS (FSYNC, AD0, SCLK, SDI, CS)						
V_{IH}, High Level Input Voltage		0.7*VDDIO			V	1
V_{IL}, Low Level Input Voltage				0.3*VDDIO	V	
C_I, Input Capacitance			< 10		pF	
DIGITAL OUTPUT (SDO, INT)						
V_{OH}, High Level Output Voltage	R_{LOAD}=1MΩ;	0.9*VDDIO			V	1
V_{OL1}, Low-Level Output Voltage	R_{LOAD}=1MΩ;			0.1*VDDIO	V	
$V_{OL.INT}$, INT Low-Level Output Voltage	OPEN=1, 0.3mA sink Current			0.1	V	
Output Leakage Current	OPEN=1		100		nA	
t_{INT}, INT Pulse Width	LATCH_INT_EN=0		50		µs	
I2C I/O (SCL, SDA)						
V_{IL}, Low-Level Input Voltage		-0.5V		0.3*VDDIO	V	1
V_{IH}, High-Level Input Voltage		0.7*VDDIO		VDDIO + 0.5V	V	
V_{hys}, Hysteresis			0.1*VDDIO		V	
V_{OL}, Low-Level Output Voltage	3mA sink current	0		0.4	V	
I_{OL}, Low-Level Output Current	V_{OL}=0.4V V_{OL}=0.6V		3 6		mA mA	
Output Leakage Current			100		nA	
t_{of}, Output Fall Time from V_{IHmax} to V_{ILmax}	C_b bus capacitance in pf	20+0.1C_b		300	ns	

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INTERNAL CLOCK SOURCE						
Sample Rate	FCHOICE_B=1,2,3 SMPLRT_DIV=0		32		kHz	2
	FCHOICE_B=0; DLPFCFG=0 or 7 SMPLRT_DIV=0		8		kHz	2
	FCHOICE_B=0; DLPFCFG=1,2,3,4,5,6; SMPLRT_DIV=0		1		kHz	2
Clock Frequency Initial Tolerance	CLK_SEL=0, 6 or gyro inactive; 25°C	-5		+5	%	1
	CLK_SEL=1,2,3,4,5 and gyro active; 25°C	-1		+1	%	1
Frequency Variation over Temperature	CLK_SEL=0,6 or gyro inactive	-10		+10	%	1
	CLK_SEL=1,2,3,4,5 and gyro active	-1		+1	%	1

Table 6. A.C. Electrical Characteristics

Notes:

1. Derived from validation or characterization of parts, not guaranteed in production.
2. Guaranteed by design.

3.3.4 Other Electrical Specifications

Typical Operating Circuit of section 0, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SERIAL INTERFACE						
SPI Operating Frequency, All Registers Read/Write	Low-Speed Characterization		100 ±10%		kHz	1
	High-Speed Characterization		1	8	MHz	1, 2
SPI Modes			Modes 0 and 3			
I^2C Operating Frequency	All registers, Fast-mode			400	kHz	1
	All registers, Standard-mode			100	kHz	1

Table 7. Other Electrical Specifications

Notes:

1. Derived from validation or characterization of parts, not guaranteed in production.
2. SPI clock duty cycle between 45% and 55% should be used for 8-MHz operation.

3.4 I2C TIMING CHARACTERIZATION

Typical Operating Circuit of section 0, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
I²C TIMING	**I²C FAST-MODE**					
f_{SCL}, SCL Clock Frequency				400	kHz	1
$t_{HD.STA}$, (Repeated) START Condition Hold Time		0.6			µs	1
t_{LOW}, SCL Low Period		1.3			µs	1
t_{HIGH}, SCL High Period		0.6			µs	1
$t_{SU.STA}$, Repeated START Condition Setup Time		0.6			µs	1
$t_{HD.DAT}$, SDA Data Hold Time		0			µs	1
$t_{SU.DAT}$, SDA Data Setup Time		100			ns	1
t_r, SDA and SCL Rise Time	C_b bus cap. from 10 to 400pF	20+0.1C_b		300	ns	1
t_f, SDA and SCL Fall Time	C_b bus cap. from 10 to 400pF	20+0.1C_b		300	ns	1
$t_{SU.STO}$, STOP Condition Setup Time		0.6			µs	1
t_{BUF}, Bus Free Time Between STOP and START Condition		1.3			µs	1
C_b, Capacitive Load for each Bus Line			< 400		pF	1
$t_{VD.DAT}$, Data Valid Time				0.9	µs	1
$t_{VD.ACK}$, Data Valid Acknowledge Time				0.9	µs	1

Table 8. I²C Timing Characteristics

Notes:

1. Based on characterization of 5 parts over temperature and voltage as mounted on evaluation board or in sockets

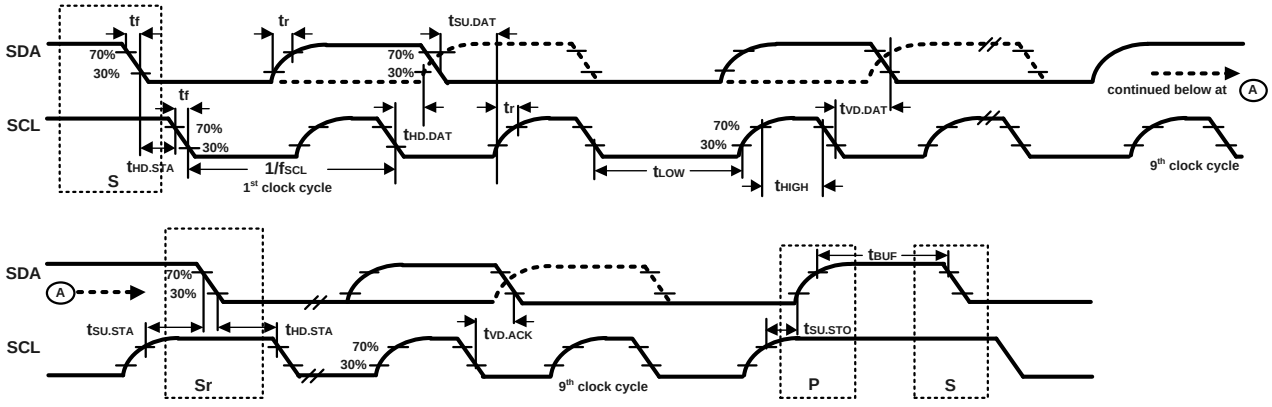

Figure 1. I2C Bus Timing Diagram

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3.5 SPI TIMING CHARACTERIZATION

Typical Operating Circuit of section 0, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SPI TIMING						
f_{SCLK}, SCLK Clock Frequency				8	MHz	1
t_{LOW}, SCLK Low Period		56			ns	1
t_{HIGH}, SCLK High Period		56			ns	1
$t_{SU.CS}$, CS Setup Time		2			ns	1
$t_{HD.CS}$, CS Hold Time		63			ns	1
$t_{SU.SDI}$, SDI Setup Time		3			ns	1
$t_{HD.SDI}$, SDI Hold Time		7			ns	1
$t_{VD.SDO}$, SDO Valid Time	C_{load} = 20pF			40	ns	1
$t_{DIS.SDO}$, SDO Output Disable Time				20	ns	1
t_{Fall}, SCLK Fall Time				6.5	ns	2
t_{Rise}, SCLK Rise Time				6.5	ns	2
$t_{DIS.SDO}$, SDO Output Disable Time				20	ns	1

Table 9. SPI Timing Characteristics (8MHz Operation)

Notes:

1. Based on characterization of 5 parts over temperature and voltage as mounted on evaluation board or in sockets
2. Based on calculation from other parameter values

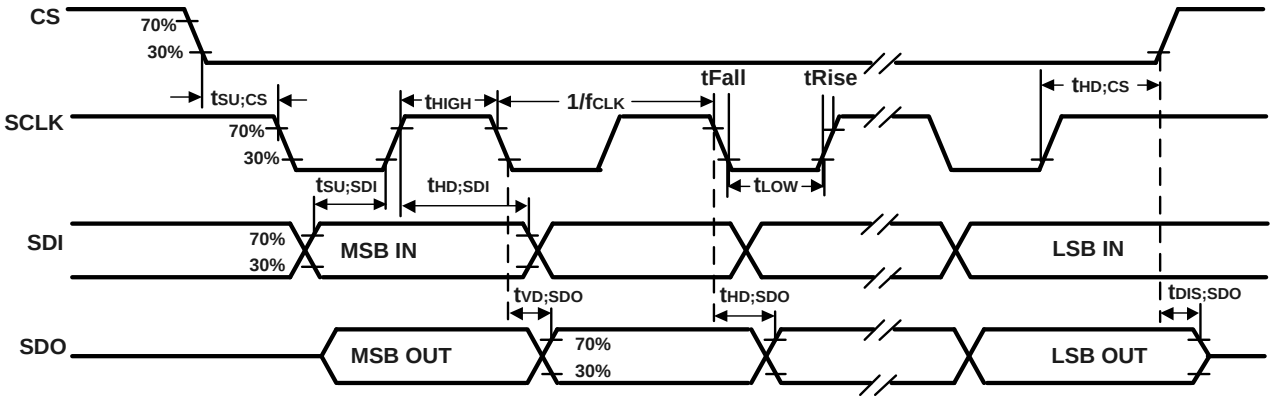

Figure 2. SPI Bus Timing Diagram

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3.6 ABSOLUTE MAXIMUM RATINGS

Stress above those listed as “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to the absolute maximum ratings conditions for extended periods may affect device reliability.

PARAMETER	RATING
Supply Voltage, VDD	-0.5V to +4V
Supply Voltage, VDDIO	-0.5V to +4V
REGOUT	-0.5V to 2V
Input Voltage Level (AD0, FSYNC, SCL, SDA)	-0.5V to VDD + 0.5V
Acceleration (Any Axis, unpowered)	10,000g for 0.2ms
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-40°C to +125°C
Electrostatic Discharge (ESD) Protection	2kV (HBM); 250V (MM)
Latch-up	JEDEC Class II (2),125°C ±100mA

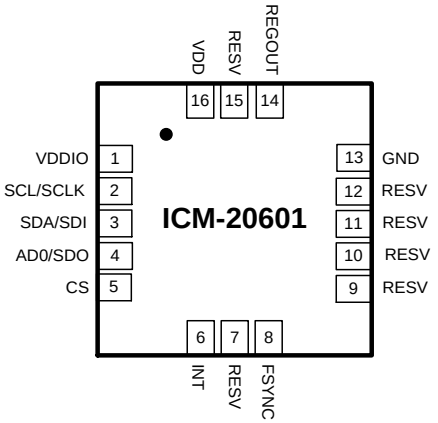
Table 10. Absolute Maximum Ratings

4. APPLICATIONS INFORMATION

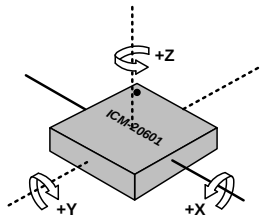
4.1 PIN OUT DIAGRAM AND SIGNAL DESCRIPTION

PIN NUMBER	PIN NAME	PIN DESCRIPTION
1	VDDIO	Digital I/O supply voltage
2	SCL/SCLK	I^2C serial clock (SCL); SPI serial clock (SCLK)
3	SDA/SDI	I^2C serial data (SDA); SPI serial data input (SDI)
4	AD0/SDO	I^2C slave address LSB (AD0); SPI serial data output (SDO)
5	CS	Chip select (0 = SPI mode; 1 = I^2C mode)
6	INT	Interrupt digital output (totem pole or open-drain)
7	RESV	Reserved. Do not connect.
8	FSYNC	Synchronization digital input (optional). Connect to GND if unused.
9	RESV	Reserved. Connect to GND.
10	RESV	Reserved. Connect to GND.
11	RESV	Reserved. Connect to GND.
12	RESV	Reserved. Connect to GND.
13	GND	Connect to GND
14	REGOUT	Regulator filter capacitor connection
15	RESV	Reserved. Connect to GND.
16	VDD	Power Supply

Table 11. Signal Descriptions



LGA Package (Top View)
16-pin, 3mm x 3mm x 0.75mm
Typical Footprint and thickness



Orientation of Axes of Sensitivity and Polarity of Rotation

Figure 3. Pin out Diagram for ICM-20601 3.0x3.0x0.75mm LGA

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4.2 TYPICAL OPERATING CIRCUIT

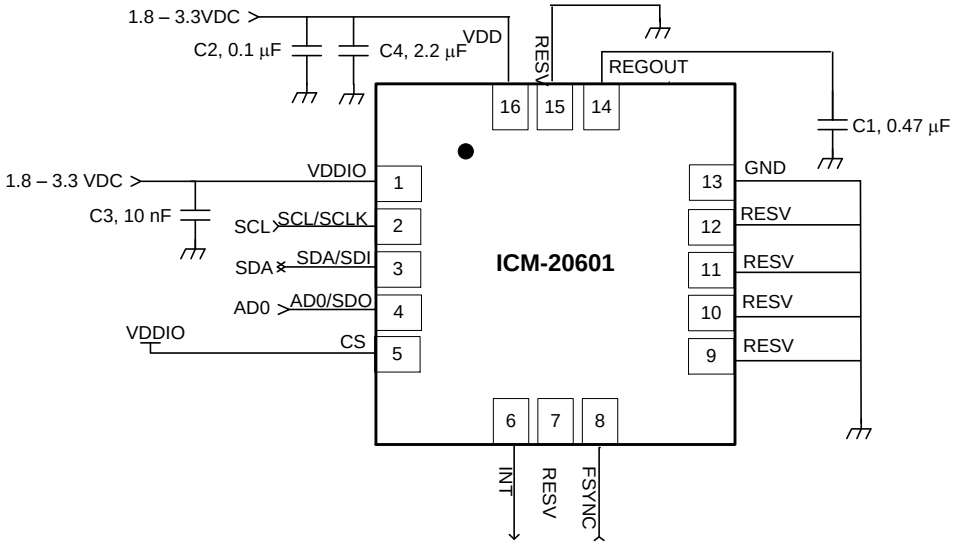

Figure 4. ICM-20601 I2C Operation Application Schematic

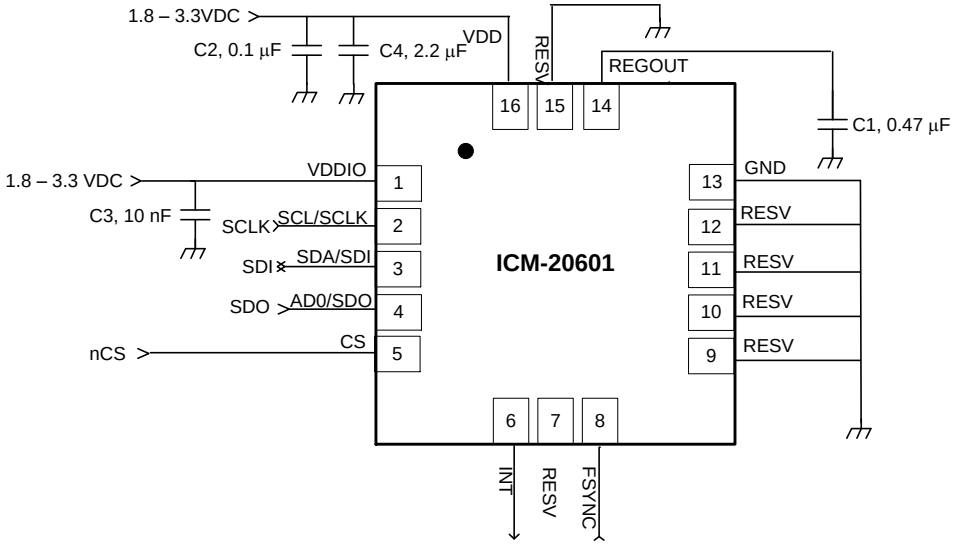

Figure 5. ICM-20601 SPI Operation Application Schematic

4.3. BILL OF MATERIALS FOR EXTERNAL COMPONENTS

COMPONENT	LABEL	SPECIFICATION	QUANTITY
REGOUT Capacitor	C1	Ceramic, X7R, 0.47µF ±10%, 2V	1
VDD Bypass Capacitors	C2	Ceramic, X7R, 0.1µF ±10%, 4V	1
	C4	Ceramic, X7R, 2.2µF ±10%, 4V	1
VDDIO Bypass Capacitor	C3	Ceramic, X7R, 10nF ±10%, 4V	1

Table 11. Bill of Materials

4.4. BLOCK DIAGRAM

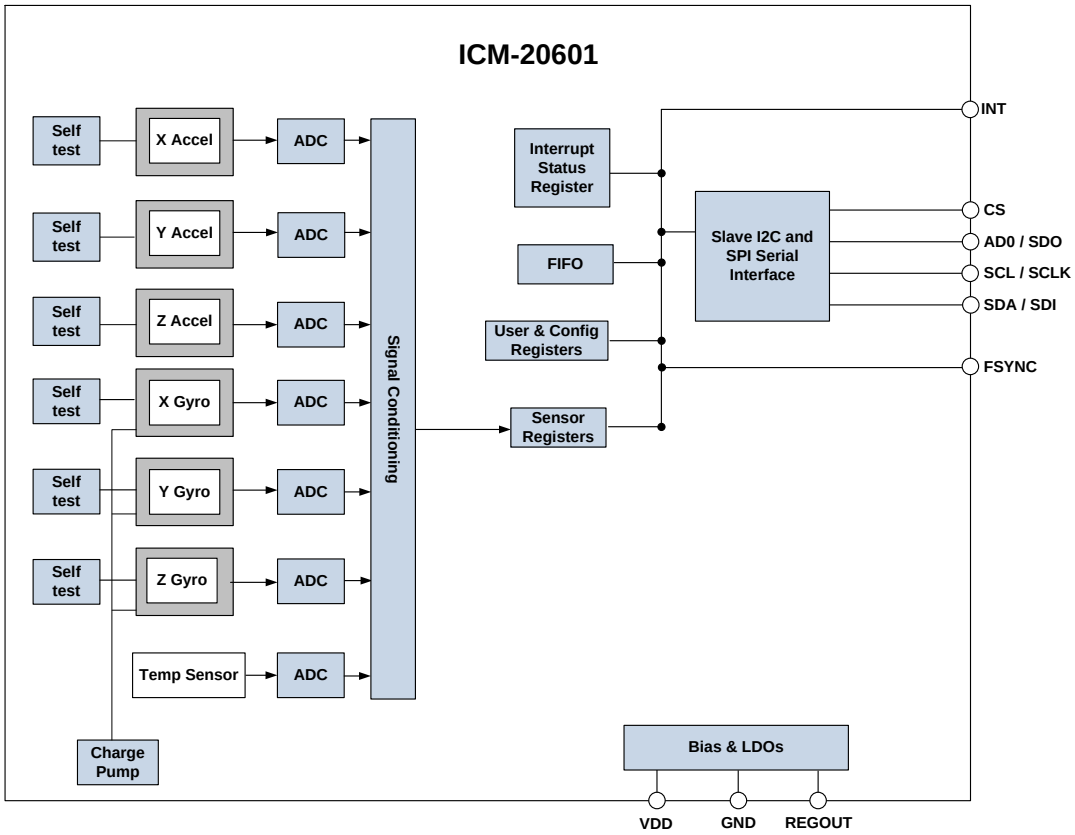

Figure 6. ICM-20601 Block Diagram

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4.5. OVERVIEW

The ICM-20601 is comprised of the following key blocks and functions:

- Three-axis MEMS rate gyroscope sensor with 16-bit ADCs and signal conditioning
- Three-axis MEMS accelerometer sensor with 16-bit ADCs and signal conditioning
- Primary I^2C and SPI serial communications interfaces
- Self-Test
- Clocking
- Sensor Data Registers
- FIFO
- Interrupts
- Digital-Output Temperature Sensor
- Bias and LDOs
- Charge Pump
- Standard Power Modes

4.6. THREE-AXIS MEMS GYROSCOPE WITH 16-BIT ADCS AND SIGNAL CONDITIONING

The ICM-20601 consists of three independent vibratory MEMS rate gyroscopes, which detect rotation about the X-, Y-, and Z- Axes. When the gyros are rotated about any of the sense axes, the Coriolis Effect causes a vibration that is detected by a capacitive pickoff. The resulting signal is amplified, demodulated, and filtered to produce a voltage that is proportional to the angular rate. This voltage is digitized using individual on-chip 16-bit Analog-to-Digital Converters (ADCs) to sample each axis. The full-scale range of the gyro sensors may be digitally programmed to ±500, ±1000, ±2000, or ±4000 degrees per second (dps). The ADC sample rate is programmable from 8,000 samples per second, down to 3.9 samples per second, and user-selectable low-pass filters enable a wide range of cut-off frequencies.

4.7. THREE-AXIS MEMS ACCELEROMETER WITH 16-BIT ADCS AND SIGNAL CONDITIONING

The ICM-20601's 3-Axis accelerometer uses separate proof masses for each axis. Acceleration along a particular axis induces displacement on the corresponding proof mass, and capacitive sensors detect the displacement differentially. The ICM-20601's architecture reduces the accelerometers' susceptibility to fabrication variations as well as to thermal drift. When the device is placed on a flat surface, it will measure 0*g* on the X- and Y-axes and +1*g* on the Z-axis. The accelerometers' scale factor is calibrated at the factory and is nominally independent of supply voltage. Each sensor has a dedicated sigma-delta ADC for providing digital outputs. The full scale range of the digital output can be adjusted to ±4*g*, ±8*g*, ±16*g*, or ±32*g*.

4.8. I2C AND SPI SERIAL COMMUNICATIONS INTERFACES

The ICM-20601 communicates to a system processor using either a SPI or an I^2C serial interface. The ICM-20601 always acts as a slave when communicating to the system processor. The LSB of the I^2C slave address is set by pin 4 (AD0).

4.8.1 ICM-20601 Solution Using I2C Interface

In the figure below, the system processor is an I^2C master to the ICM-20601.

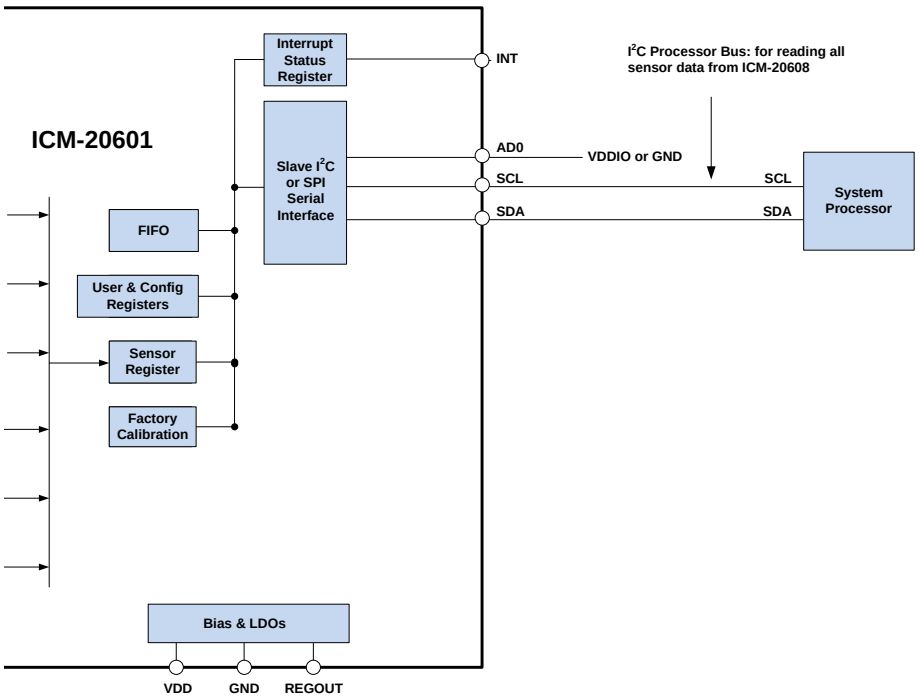

Figure 7. ICM-20601 Solution Using I²C Interface

4.8.2 ICM-20601 Solution Using SPI Interface

In the figure below, the system processor is an SPI master to the ICM-20601. Pins 2, 3, 4, and 5 are used to support the SCLK, SDI, SDO, and CS signals for SPI communications.

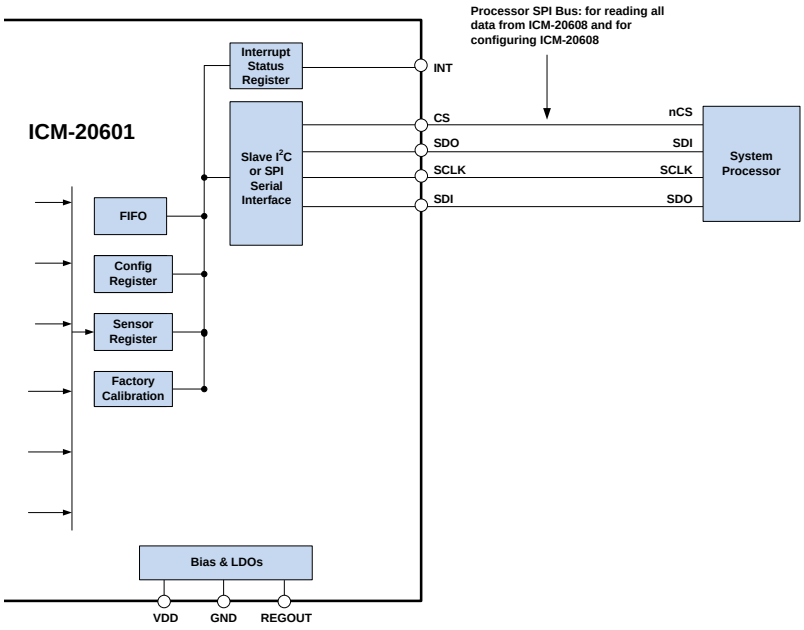

Figure 8. ICM-20601 Solution Using SPI Interface

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4.9 SELF-TEST

Self-test allows for the testing of the mechanical and electrical portions of the sensors. The self-test for each measurement axis can be activated by means of the gyroscope and accelerometer self-test registers (registers 27 and 28).

When the self-test is activated, the electronics cause the sensors to be actuated and produce an output signal. The output signal is used to observe the self-test response.

The self-test response is defined as follows:

Self-test response = Sensor output with self-test enabled – Sensor output with self-test disabled

The self-test response for each gyroscope axis is defined in the gyroscope specification table, while that for each accelerometer axis is defined in the accelerometer specification table.

When the value of the self-test response is within the specified min/max limits of the product specification, the part has passed self-test. When the self-test response exceeds the min/max values, the part is deemed to have failed self-test. It is recommended to use InvenSense MotionApps software for executing self-test.

4.10 CLOCKING

The ICM-20601 has a flexible clocking scheme, allowing a variety of internal clock sources to be used for the internal synchronous circuitry. This synchronous circuitry includes the signal conditioning and ADCs, and various control circuits and registers. An on-chip PLL provides flexibility in the allowable inputs for generating this clock.

Allowable internal sources for generating the internal clock are:

a) An internal relaxation oscillator
b) Auto-select between internal relaxation oscillator and gyroscope MEMS oscillator to use the best available source

The only setting supporting specified performance in all modes is option b). It is recommended that option b) be used.

4.11 SENSOR DATA REGISTERS

The sensor data registers contain the latest gyroscope, accelerometer, and temperature measurement data. They are read-only registers, and are accessed via the serial interface. Data from these registers may be read anytime.

4.12 FIFO

The ICM-20601 contains a 512-byte FIFO register that is accessible via the Serial Interface. The FIFO configuration register determines which data is written into the FIFO. Possible choices include gyro data, accelerometer data, temperature readings, and FSYNC input. A FIFO counter keeps track of how many bytes of valid data are contained in the FIFO. The FIFO register supports burst reads. The interrupt function may be used to determine when new data is available.
The ICM-20601 allows FIFO read in standard (duty cycle) accelerometer mode.

4.13 INTERRUPTS

Interrupt functionality is configured via the Interrupt Configuration register. Items that are configurable include the INT pin configuration, the interrupt latching and clearing method, and triggers for the interrupt. Items that can trigger an interrupt are (1) Clock generator locked to new reference oscillator (used when switching clock sources); (2) new data is available to be read (from the FIFO and Data registers); (3) accelerometer event interrupts; (4) FIFO overflow. The interrupt status can be read from the Interrupt Status register.

4.14 DIGITAL-OUTPUT TEMPERATURE SENSOR

An on-chip temperature sensor and ADC are used to measure the ICM-20601 die temperature. The readings from the ADC can be read from the FIFO or the Sensor Data registers.

4.15 BIAS AND LDOS

The bias and LDO section generates the internal supply and the reference voltages and currents required by the ICM-20601. Its two inputs are an unregulated VDD and a VDDIO logic reference supply voltage. The LDO output is bypassed by a capacitor at REGOUT. For further details on the capacitor, please refer to the Bill of Materials for External Components.

4.16 CHARGE PUMP

An on-chip charge pump generates the high voltage required for the MEMS oscillator.

4.17 POWER MODES

The following table lists the user-accessible power modes for ICM-20601.

MODE	NAME	GYRO	ACCEL
1	Sleep Mode	Off	Off
2	Standby Mode	Drive On	Off
3	Accelerometer Standard Mode	Off	Duty-Cycled
4	Accelerometer Low-Noise Mode	Off	On
5	Gyroscope Standard Mode	Duty-Cycled	Off
6	Gyroscope Low-Noise Mode	On	Off
7	6-Axis Low-Noise Mode	On	On
8	6-Axis Standard Mode	Duty-Cycled	On

Table 12. Power Modes for ICM-20601

5 PROGRAMMABLE INTERRUPTS

The ICM-20601 has a programmable interrupt system which can generate an interrupt signal on the INT pin. Status flags indicate the source of an interrupt. Interrupt sources may be enabled and disabled individually.

INTERRUPT NAME	MODULE
Motion Detection	Motion
FIFO Overflow	FIFO
Data Ready	Sensor Registers

Table 13. Table of Interrupt Sources

5.1 WAKE-ON-MOTION INTERRUPT

The ICM-20601 provides motion detection capability. A qualifying motion sample is one where the high passed sample from any axis has an absolute value exceeding a user-programmable threshold. The following steps explain how to configure the Wake-on-Motion Interrupt.

Step 1: Ensure that Accelerometer is running

- In PWR_MGMT_1 register (0x6B) set CYCLE = 0, SLEEP = 0, and GYRO_STANDBY = 0
- In PWR_MGMT_2 register (0x6C) set STBY_XA = STBY_YA = STBY_ZA = 0, and STBY_XG = STBY_YG = STBY_ZG = 1

Step 2: Accelerometer Configuration

- In ACCEL_CONFIG2 register (0x1D) set ACCEL_FCHOICE_B = 0 and A_DLPF_CFG[2:0] = 1 (b001)

Step 3: Enable Motion Interrupt

- In INT_ENABLE register (0x38) set WOM_INT_EN = 111 to enable motion interrupt

Step 4: Set Motion Threshold

- Set the motion threshold in ACCEL_WOM_THR register (0x1F)

Step 5: Enable Accelerometer Hardware Intelligence

- In ACCEL_INTEL_CTRL register (0x69) set ACCEL_INTEL_EN = ACCEL_INTEL_MODE = 1; Ensure that bit 0 is set to 0.

Step 6: Set Frequency of Wake-Up

- In Standard Mode Configuration register (0x1E) set LPOSC_CLKSEL[3:0] for a sample rate as indicated in the register map

Step 7: Enable Cycle Mode (Accelerometer Standard Mode)

- In PWR_MGMT_1 register (0x6B) set CYCLE = 1

6 DIGITAL INTERFACE

6.1 I2C AND SPI SERIAL INTERFACES

The internal registers and memory of the ICM-20601 can be accessed using either I^2C at 400 kHz or SPI at 8MHz. SPI operates in four-wire mode.

PIN NUMBER	PIN NAME	PIN DESCRIPTION
1	VDDIO	Digital I/O supply voltage.
4	AD0 / SDO	I^2C Slave Address LSB (AD0); SPI serial data output (SDO)
2	SCL / SCLK	I^2C serial clock (SCL); SPI serial clock (SCLK)
3	SDA / SDI	I^2C serial data (SDA); SPI serial data input (SDI)

Table 14. Serial Interface

Note:
To prevent switching into I^2C mode when using SPI, the I^2C interface should be disabled by setting the *I2C_IF_DIS* configuration bit. Setting this bit should be performed immediately after waiting for the time specified by the "Start-Up Time for Register Read/Write" in Section 3.3.3.

6.2 I2C INTERFACE

I^2C is a two-wire interface comprised of the signals serial data (SDA) and serial clock (SCL). In general, the lines are open-drain and bi-directional. In a generalized I^2C interface implementation, attached devices can be a master or a slave. The master device puts the slave address on the bus, and the slave device with the matching address acknowledges the master.

The ICM-20601 always operates as a slave device when communicating to the system processor, which thus acts as the master. SDA and SCL lines typically need pull-up resistors to VDD. The maximum bus speed is 400 kHz.

The slave address of the ICM-20601 is b110100X which is 7 bits long. The LSB bit of the 7 bit address is determined by the logic level on pin AD0. This allows two ICM-20601s to be connected to the same I^2C bus. When used in this configuration, the address of one of the devices should be b1101000 (pin AD0 is logic low) and the address of the other should be b1101001 (pin AD0 is logic high).

6.3 I2C COMMUNICATIONS PROTOCOL

START (S) and STOP (P) Conditions
Communication on the I^2C bus starts when the master puts the START condition (S) on the bus, which is defined as a HIGH-to-LOW transition of the SDA line while SCL line is HIGH (see figure below). The bus is considered to be busy until the master puts a STOP condition (P) on the bus, which is defined as a LOW to HIGH transition on the SDA line while SCL is HIGH (see figure below). Additionally, the bus remains busy if a repeated START (Sr) is generated instead of a STOP condition.

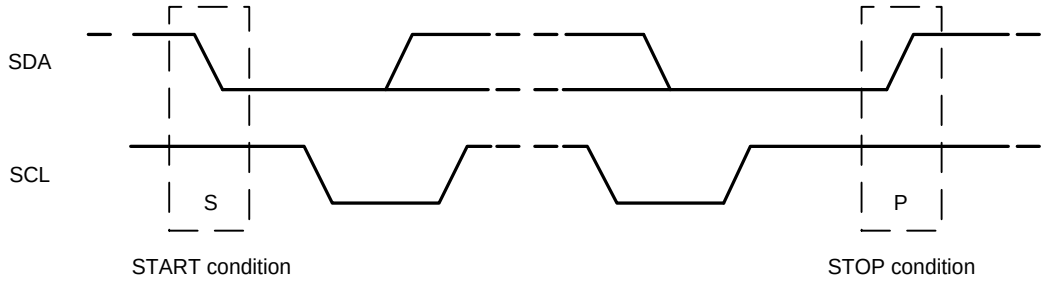

Figure 9. START and STOP Conditions

Data Format / Acknowledge

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I^2C data bytes are defined to be 8-bits long. There is no restriction to the number of bytes transmitted per data transfer. Each byte transferred must be followed by an acknowledge (ACK) signal. The clock for the acknowledge signal is generated by the master, while the receiver generates the actual acknowledge signal by pulling down SDA and holding it low during the HIGH portion of the acknowledge clock pulse.

If a slave is busy and cannot transmit or receive another byte of data until some other task has been performed, it can hold SCL LOW, thus forcing the master into a wait state. Normal data transfer resumes when the slave is ready, and releases the clock line (refer to the following figure).

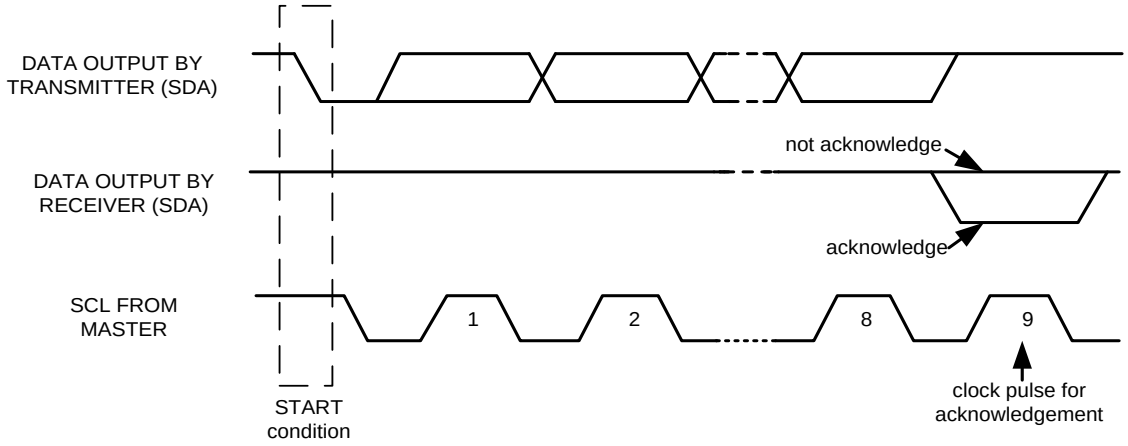


Figure 10. Acknowledge on the I^2C Bus

Communications

After beginning communications with the START condition (S), the master sends a 7-bit slave address followed by an 8th bit, the read/write bit. The read/write bit indicates whether the master is receiving data from or is writing to the slave device. Then, the master releases the SDA line and waits for the acknowledge signal (ACK) from the slave device. Each byte transferred must be followed by an acknowledge bit. To acknowledge, the slave device pulls the SDA line LOW and keeps it LOW for the high period of the SCL line. Data transmission is always terminated by the master with a STOP condition (P), thus freeing the communications line. However, the master can generate a repeated START condition (Sr), and address another slave without first generating a STOP condition (P). A LOW to HIGH transition on the SDA line while SCL is HIGH defines the stop condition. All SDA changes should take place when SCL is low, with the exception of start and stop conditions.

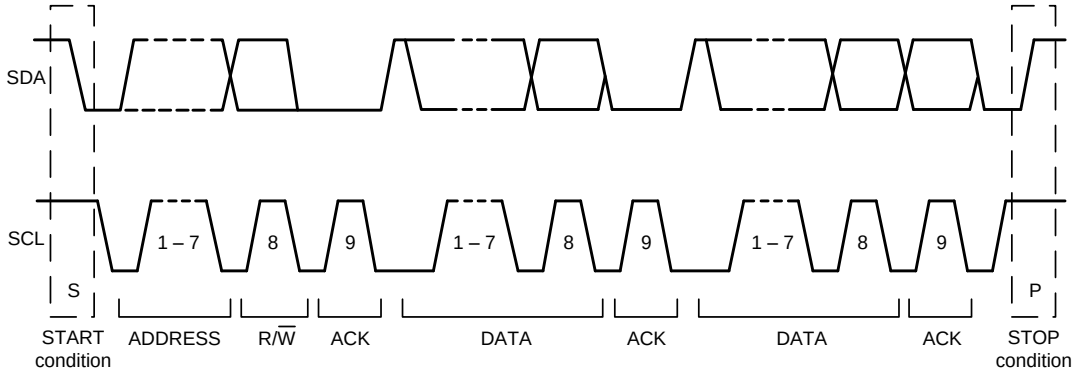


Figure 11. Complete I^2C Data Transfer

To write the internal ICM-20601 registers, the master transmits the start condition (S), followed by the I^2C address and the write bit (0). At the 9th clock cycle (when the clock is high), the ICM-20601 acknowledges the transfer. Then the master puts the register address (RA) on the bus. After the ICM-20601 acknowledges the reception of the register address, the master puts the register data onto the bus. This is followed by the ACK signal, and data transfer may be concluded by the stop condition (P). To write multiple bytes after the last ACK signal, the master can continue outputting data rather than transmitting a stop signal. In this case, the ICM-20601 automatically increments the register address and loads the data to the appropriate register. The following figures show single and two-byte write sequences.

Single-Byte Write Sequence

Master	S	AD+W		RA		DATA		P
Slave			ACK		ACK		ACK	

Burst Write Sequence

Master	S	AD+W		RA		DATA		DATA		P
Slave			ACK		ACK		ACK		ACK	

To read the internal ICM-20601 registers, the master sends a start condition, followed by the I^2C address and a write bit, and then the register address that is going to be read. Upon receiving the ACK signal from the ICM-20601, the master transmits a start signal followed by the slave address and read bit. As a result, the ICM-20601 sends an ACK signal and the data. The communication ends with a not acknowledge (NACK) signal and a stop bit from master. The NACK condition is defined such that the SDA line remains high at the 9th clock cycle. The following figures show single and two-byte read sequences.

Single-Byte Read Sequence

Master	S	AD+W		RA		S	AD+R			NACK	P
Slave			ACK		ACK			ACK	DATA		

Burst Read Sequence

Master	S	AD+W		RA		S	AD+R			ACK		NACK	P
Slave			ACK		ACK			ACK	DATA		DATA		

6.4 I^2C TERMS

SIGNAL	DESCRIPTION
S	Start Condition: SDA goes from high to low while SCL is high
AD	Slave I^2C address
W	Write bit (0)
R	Read bit (1)
ACK	Acknowledge: SDA line is low while the SCL line is high at the 9th clock cycle
NACK	Not-Acknowledge: SDA line stays high at the 9th clock cycle
RA	ICM-20601 internal register address
DATA	Transmit or received data
P	Stop condition: SDA going from low to high while SCL is high

Table 15. I^2C Terms

6.5 SPI INTERFACE

SPI is a 4-wire synchronous serial interface that uses two control lines and two data lines. The ICM-20601 always operates as a Slave device during standard Master-Slave SPI operation.

With respect to the Master, the Serial Clock output (SCLK), the Serial Data Output (SDO) and the Serial Data Input (SDI) are shared among the Slave devices. Each SPI slave device requires its own Chip Select (CS) line from the master.

CS goes low (active) at the start of transmission and goes back high (inactive) at the end. Only one CS line is active at a time, ensuring that only one slave is selected at any given time. The CS lines of the non-selected slave devices are held high, causing their SDO lines to remain in a high-impedance (high-z) state so that they do not interfere with any active devices.

SPI Operational Features

1. Data is delivered MSB first and LSB last
2. Data is latched on the rising edge of SCLK
3. Data should be transitioned on the falling edge of SCLK
4. The maximum frequency of SCLK is 8MHz
5. SPI read and write operations are completed in 16 or more clock cycles (two or more bytes). The first byte contains the SPI Address, and the following byte(s) contain(s) the SPI data. The first bit of the first byte contains the Read/Write bit and indicates the Read (1) or Write (0) operation. The following 7 bits contain the Register Address. In cases of multiple-byte Read/Writes, data is two or more bytes:

SPI Address format

MSB							**LSB**
R/W	A6	A5	A4	A3	A2	A1	A0

SPI Data format

MSB							**LSB**
D7	D6	D5	D4	D3	D2	D1	D0

6. Supports Single or Burst Read/Writes.

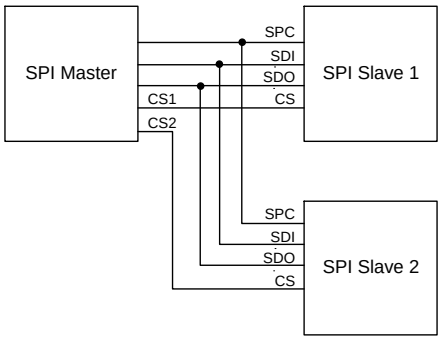


Figure 12. Typical SPI Master/Slave Configuration

7 ASSEMBLY

This section provides general guidelines for assembling InvenSense Micro Electro-Mechanical Systems (MEMS) gyros packaged in LGA package.

ORIENTATION OF AXES

The diagram below shows the orientation of the axes of sensitivity and the polarity of rotation. Note the pin 1 identifier (•) in the figure.

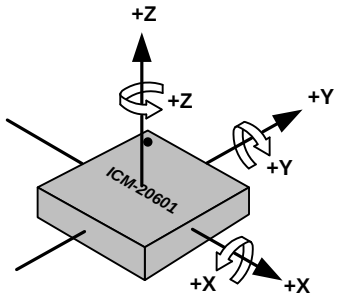
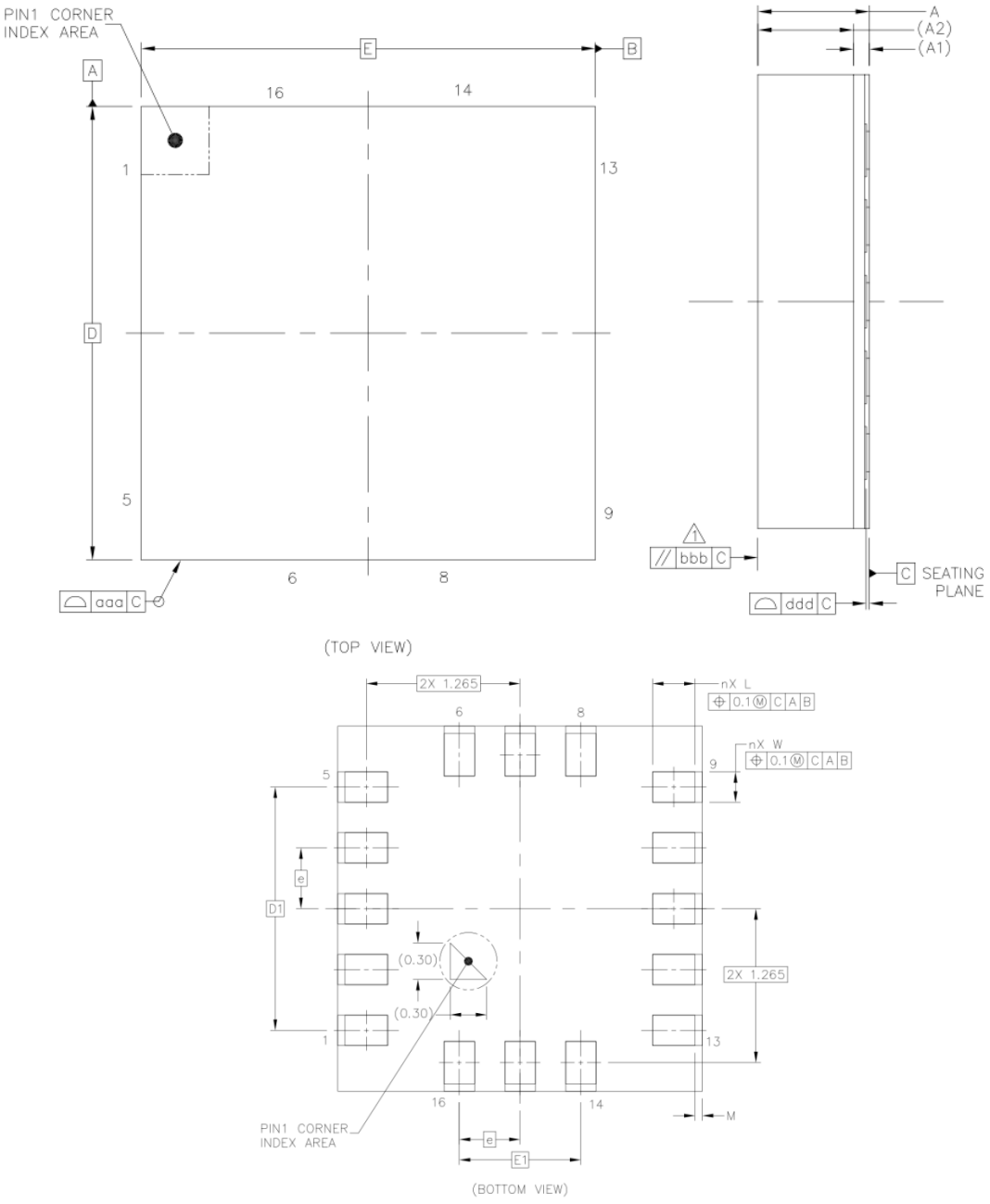


Figure 13. Orientation of Axes of Sensitivity and Polarity of Rotation

PACKAGE DIMENSIONS

16 Lead LGA (3x3x0.75) mm NiAu pad finish



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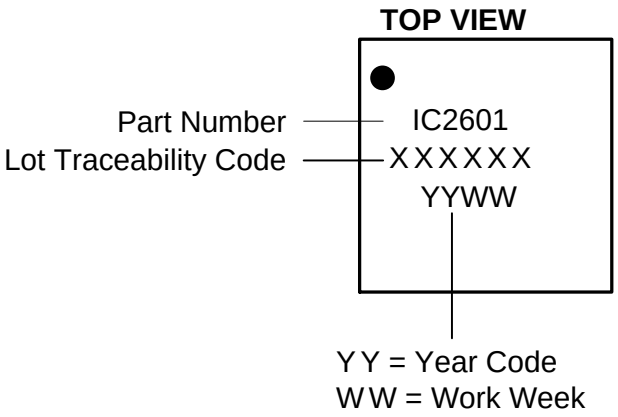
	SYMBOLS	DIMENSIONS IN MILLIMETERS		
		MIN	NOM	MAX
Total Thickness	A	0.7	0.75	0.8
Substrate Thickness	A1		0.105	REF
Mold Thickness	A2		0.63	REF
Body Size	D	2.9	3	3.1
	E	2.9	3	3.1
Lead Width	W	0.2	0.25	0.3
Lead Length	L	0.3	0.35	0.4
Lead Pitch	e		0.5	BSC
Lead Count	n		16	
Edge Ball Center to Center	D1		2	BSC
	E1		1	BSC
Body Center to Contact Ball	SD		---	BSC
	SE		---	BSC
Ball Width	b	---	---	---
Ball Diameter			---	
Ball Opening			---	
Ball Pitch	e1		---	
Ball Count	n1		---	
Pre-Solder		---	---	---
Package Edge Tolerance	aaa		0.1	
Mold Flatness	bbb		0.2	
Coplanarity	ddd		0.08	
Ball Offset (Package)	eee		---	
Ball Offset (Ball)	fff		---	
Lead Edge to Package Edge	M	0.01	0.06	0.11

8 PART NUMBER PACKAGE MARKING

The part number package marking for ICM-20601 devices is summarized below:

PART NUMBER	PART NUMBER PACKAGE MARKING
ICM-20601	IC2601



9 REFERENCE

Please refer to “InvenSense MEMS Handling Application Note (AN-IVS-0002A-00)” for the following information:

- Manufacturing Recommendations
    - Assembly Guidelines and Recommendations
    - PCB Design Guidelines and Recommendations
    - MEMS Handling Instructions
    - ESD Considerations
    - Reflow Specification
    - Storage Specifications
    - Package Marking Specification
    - Tape & Reel Specification
    - Reel & Pizza Box Label
    - Packaging
    - Representative Shipping Carton Label
- Compliance
    - Environmental Compliance
    - DRC Compliance
    - Compliance Declaration Disclaimer

REVISION HISTORY

REVISION DATE	REVISION NUMBER	DESCRIPTION
06/03/2015	1.0	Initial Release

COMPLIANCE DECLARATION DISCLAIMER

InvenSense believes the environmental and other compliance information given in this document to be correct but cannot guarantee accuracy or completeness. Conformity documents substantiating the specifications and component characteristics are on file. InvenSense subcontracts manufacturing and the information contained herein is based on data received from vendors and suppliers, which has not been validated by InvenSense.

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