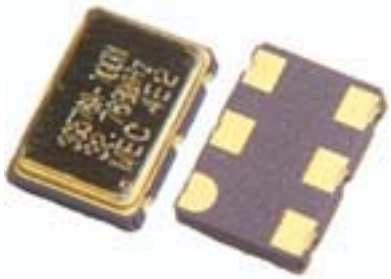
3HP5761, features less than 1 ps RMS phase jitter from non-PLL circuitry. Its extremely low phase noise and jitter makes 3HP5761 ideal for SONET and other communication protocols. RoHS compliant and Pb free packaging. Pad 1 is used to Tri-state PECL and complimentary PECL outputs.



General Specifications

Product Series		**3HP5761**				
Frequency Range		60 MHz ~ 800 MHz. Non-PLL based.				
Output Logic		Differential PECL 100 K square wave				
Frequency Stability Commercial temp. range (code "**C**") Industrial temp. range (code "**I**")		"**A**": ±25 ppm over 0°C to +70°C "**B**":±50 ppm over 0°C to +70°C "**C**":±100 ppm over 0°C to +70°C For non-standard please specify desired frequency stability after the "C". For example "C20" is ±20 ppm over 0 to +70°C				
		"**D**":±25 ppm over -40°C to +85° (not available on all packages) "**E**":±50 ppm over -40°C to +85°C "**F**":±100 ppm over -40°C to +85°C For non-standard please give desired frequency stability after the "**I**". For example "I20" is ±20 ppm over -40 to +85°C				
		vs ±10% supply voltage change:±3 ppm max. vs ±10% Load change: ±2 ppm max.				
Supply Voltage V_{DD}		+3.3 V ± 10 %				
Output Voltage HIGH "1", V_{OH}		V_{DD}-1.025 V min.; V_{DD}-0.880 V max. Condition: RL=50 ohms to V_{DD}-2V				
Output Voltage LOW "0", V_{OL}		V_{DD}-1.810 V min..; V_{DD}-1.620 V max. Condition: RL=50 ohms to V_{DD}-2V				
Current Consumption		75 mA max. for 212.50 MHz 80 mA max. for 622.080 MHz				
Load		50 ohms into V_{DD}-2V or Thevenin equivalent. (terminating resistors required on all outputs)				
Rise Time (Tr) and Fall Time (Tf)		0.25 nano sec. typical; 0.50 nano sec. max (20% ↔ 80%)				
Duty Cycle		50% ± 5% max. measured at V_{DD} -1.3V				
Phase Jitter (RMS)		1 ps max. (12 KHz to 20 MHz)				
Period Jitter (RMS)		**155.520 MHz**		**311.04 MHz**		**622.080 MHz**	
		typical	max.	typical	max.	typical	max.
		2.5 ps	3 ps	2.5 ps	3 ps	4 ps	6 ps
Period Jitter (Peak-to-Peak)		21 ps	30 ps	18 ps	20 ps	25 ps	30 ps
Accumulated Jitter (RMS)			5 ps		4 ps		6 ps
Phase Noise **(offset from carrier)**	**10 Hz Offset**	-72 dBc/ Hz		-60 dBc/ Hz		-55 dBc/ Hz	
	100 Hz Offset	-100 dBc/ Hz		-92 dBc/ Hz		-85 dBc/ Hz	
	1 KHz Offset	-125 dBc/ Hz		-122 dBc/ Hz		-110 dBc/ Hz	
	10 KHz Offset	-132 dBc/ Hz		-140 dBc/ Hz		-130 dBc/ Hz	
	100 KHz Offset	-142 dBc/ Hz		-142 dBc/ Hz		-137 dBc/ Hz	
	1 MHz Offset	-147 dBc/ Hz		-146 dBc/ Hz		-148 dBc/ Hz	
	10 MHz Offset	-149 dBc/ Hz		-146 dBc/ Hz		-150 dBc/ Hz	
Start-up Time		10 m sec. max.					
Aging		±2 ppm / year max.					

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U.S.A.: TEL (1)-909-466-0427, FAX (1)-909-466-0762, e-mail: sales-us@mercury-crystal.com

Tri-state option on pad No. 1	**No Connection**	PECL and complimentary PECL outputs.
	Disable	Both outputs are disabled (high impedance) when pad No. 1 is taken below 0.3 Vcc referenced to ground. Oscillator is always ON. Special request: Oscillator is off when disabled. Contact Mercury.
	Enable	At disabled mode, both outputs are enabled when pad No. 1 is taken above 0.7 Vcc referenced to ground.
Input Static Discharge Protection		2 KV max.
Absolute Maximum Rating (permanent damage may be created if operate beyond limits specified)		
Supply Voltage V_{DD}		+4.6 V D.C. max.
Input Voltage Vi		Vss-0.5V min.; V_{DD} +0.5V max.
Input Voltage Vo		Vss-0.5V min.; V_{DD} +0.5V max.
Storage Temperature Ts		-55°C min.; +150°C max.

(1)Inclusive of 25°C tolerance, operating temperature range, ±10% input voltage variation, load change, aging at +25°C, shock and vibration.

Environmental Performance Specifications

Green Requirement	RoHS Compliant and Pb (lead) free
Storage temp. range	-55 to +125°C
Humidity	85% RH, 85°C, 48 hours
Hermetic seal	Leak rate $2x10^{-8}$ ATM-cm^3/sec max.
Solderability	MIL-STD-202F method 208E
Reflow	260°C for 10 sec.
Vibration	MIL-STD-202F method 204, 35G, 50 to 2000 Hz
Shock	MIL-STD-202F method 213B, test condi. E, 1000GG ½ sine wave

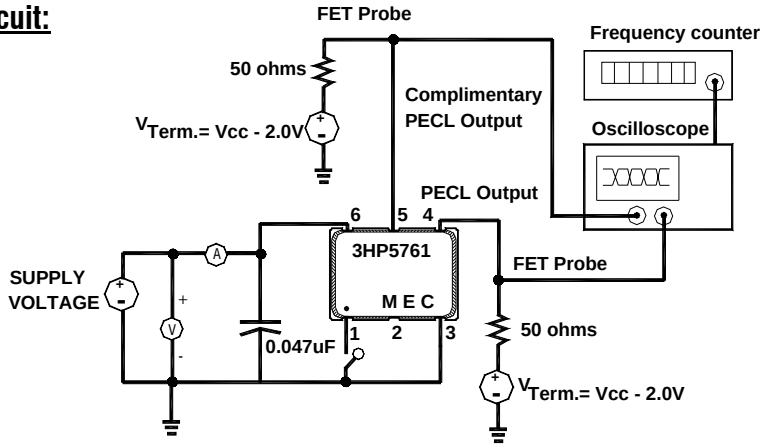
Part Number Format and Example:

Example: 3HP5761-A-155.520
Explanation: HP5761 PECL clock oscillator, 5x7 mm SMD package with pad 1 as Tri-state, +3.3 V supply voltage, ±25 ppm frequency stability over 0 to +70°C, 155.520 MHz, non-PLL based

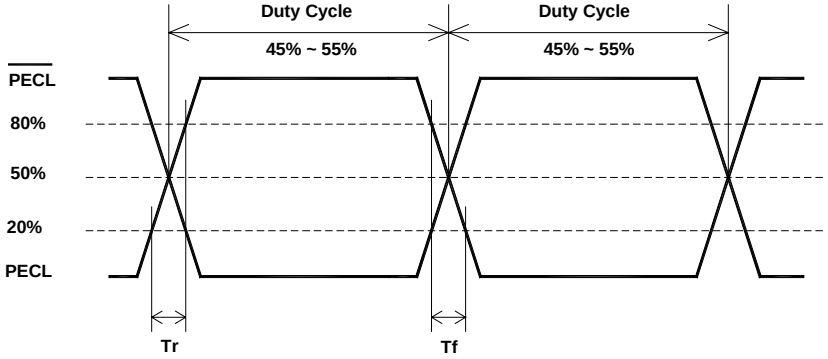
			✍		✍	✍: customer to specify
3	HP5761	—	A	—	155.520	
❶	❷		❸		❹	

❶: Voltage codes: "**3**" for +3.3 V
❷: HP5761 product series ❸: Frequency stability code: "**A**" ~ "**F**" or custom. See table above.
❹: Frequency in MHz

HP5761 Test Circuit:

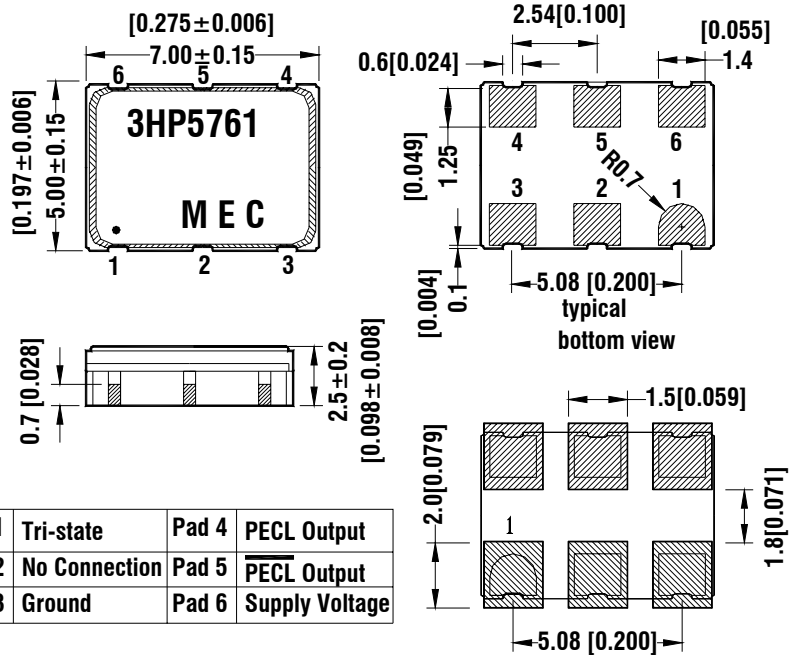


HP5761 OUTPUT WAVEFORM:



HP5761 Package Dimensions and Recommended Pad Layout:

unit mm[inches]



Pad 1	Tri-state	Pad 4	PECL Output
Pad 2	No Connection	Pad 5	$\overline{\text{PECL}}$ Output
Pad 3	Ground	Pad 6	Supply Voltage

Chamfered pad is pad No. 1. Count counter-clockwise when looking at top view.
Count clockwise when looking at bottom view.