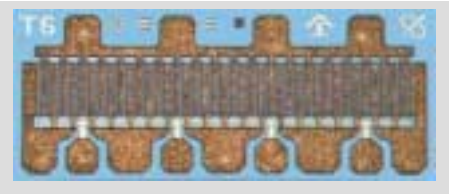
2W High Linearity and High Efficiency GaAs Power FETs

FEATURES

- 2W Typical Power at 6 GHz
- Linear Power Gain: G_L = 12 dB Typical at 6 GHz
- High Linearity: IP3 = 43 dBm Typical at 6 GHz
- Via Hole Source Ground
- Suitable for High Reliability Application
- Breakdown Voltage: $BV_{DGO} \geq 18$ V
- Lg = 0.6 μm, Wg = 5 mm
- High Power Added Efficiency: Nominal PAE of 43 % at 6 GHz
- Tight Vp ranges control
- High RF input power handling capability
- 100 % DC Tested

PHOTO ENLARGEMENT



DESCRIPTION

The TC1606 is a GaAs Pseudomorphic High Electron Mobility Transistor (PHEMT) which has high linearity and high Power Added Efficiency. The device is processed with a propriety via-hole process, which provides low thermal resistance and low inductance. The long gate length makes the device to have high breakdown voltage. All devices are 100% DC tested to assure consistent quality. Bond pads are gold plated for either thermo-compression or thermo-sonic wire bonding. Backside gold plating is compatible with standard AuSn die-attach. Typical application include commercial and military high performance power amplifiers

ELECTRICAL SPECIFICATIONS (T_A=25 °C)

Symbol	Conditions	MIN	TYP	MAX	UNIT
P_{1dB}	Output Power at 1dB Gain Compression Point , f = 6 GHz V_{DS} = 8 V, I_{DS} = 500 mA	32.5	33		dBm
G_L	Linear Power Gain, f = 6 GHz V_{DS} = 8 V, I_{DS} = 500 mA	11	12		dB
IP3	Intercept Point of the 3rd-order Intermodulation, f = 6 GHz V_{DS} = 8 V, I_{DS} = 500 mA,*P_{SCL} = 20 dBm		43		dBm
PAE	Power Added Efficiency at 1dB Compression Power, f = 6 GHz		43		%
I_{DSS}	Saturated Drain-Source Current at V_{DS} = 2 V, V_{GS} = 0 V		1.2		A
g_m	Transconductance at V_{DS} = 2 V, V_{GS} = 0 V		850		mS
V_P	Pinch-off Voltage at V_{DS} = 2 V, I_D = 10 mA		-1.7**		Volts
BV_{DGO}	Drain-Gate Breakdown Voltage at I_{DGO} = 2.5 mA	18	22		Volts
R_{th}	Thermal Resistance		6		°C/W

Note:

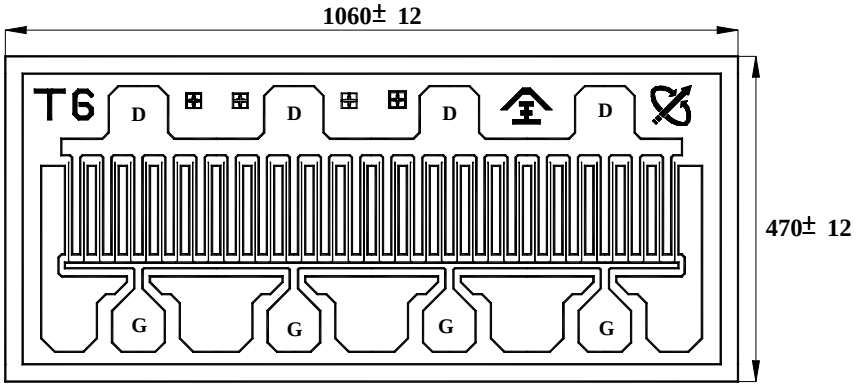
*** P_{SCL}: Output Power of Single Carrier Level.**

* *For the tight control of the pinch-off voltage . TC1606's are divided into 3 groups:
(1)**TC1606P1519** : Vp = -1.5V to -1.9V (2) **TC1606P1620** : Vp = -1.6V to -2.0V
(3)**TC1606P1721** : Vp = -1.7V to -2.1V In addition, the customers may specify their requirements.

ABSOLUTE MAXIMUM RATINGS (T_A=25 °C)

Symbol	Parameter	Rating
V_{DS}	Drain-Source Voltage	12 V
V_{GS}	Gate-Source Voltage	-5 V
I_{DS}	Drain Current	I_{DSS}
P_{in}	RF Input Power, CW	30 dBm
P_T	Continuous Dissipation	7.7 W
T_{CH}	Channel Temperature	175 °C
T_{STG}	Storage Temperature	- 65 °C to +175 °C

CHIP DIMENSIONS



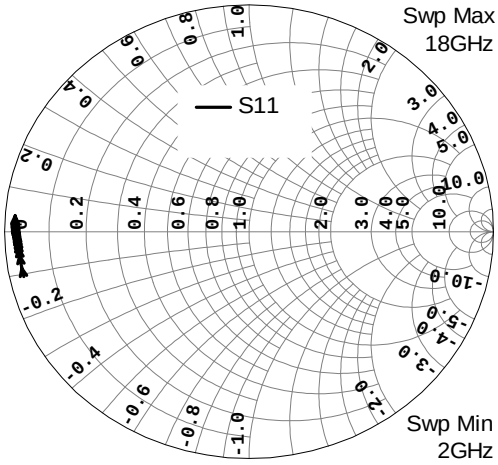
Units: Micrometers

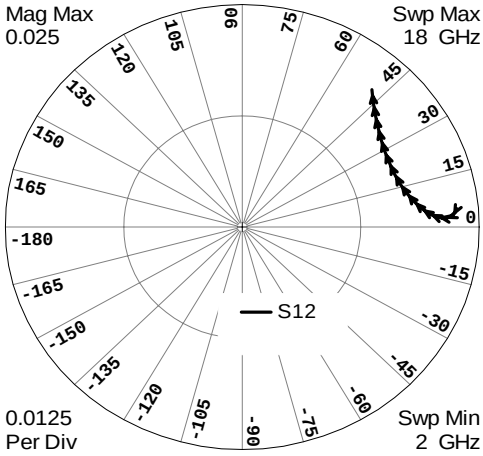
Chip Thickness: 50

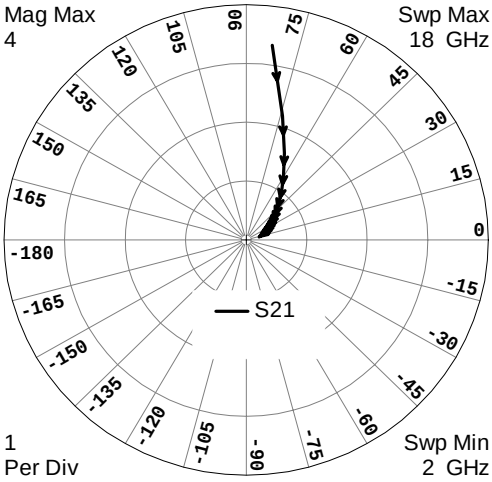
Gate Pad: 76 x 59.5

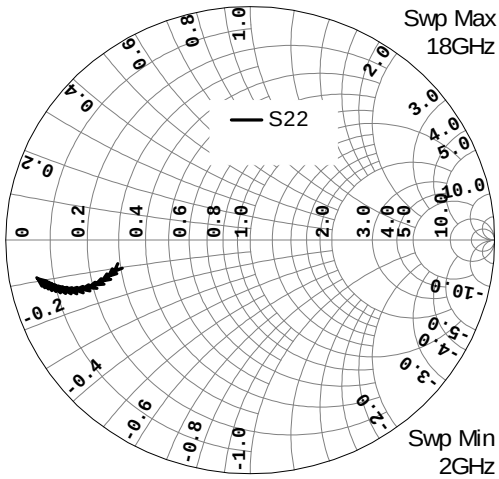
Drain Pad: 86.0 x 76.0

TYPICAL SCATTERING PARAMETERS (T_A=25 °C) V_{DS} = 8 V, I_{DS} = 500 mA







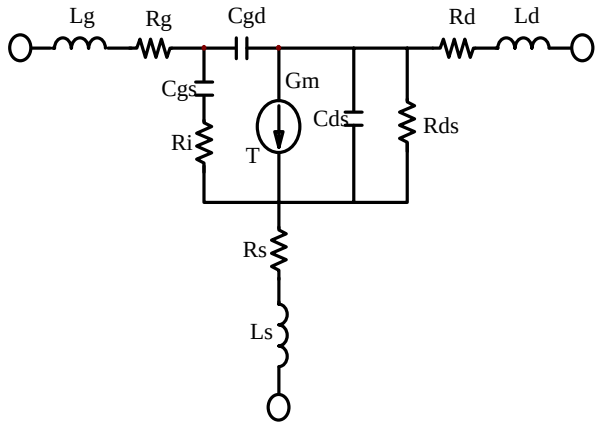


FREQUENCY	S11		S21		S12		S22	
(GHz)	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
2	0.9431	-167.86	3.3354	82.58	0.0227	5.17	0.5586	-167.33
3	0.9438	-172.26	2.1882	74.07	0.0222	3.12	0.5845	-165.78
4	0.9450	-174.61	1.6019	66.85	0.0215	2.57	0.6143	-164.36
5	0.9464	-176.14	1.2440	60.39	0.0206	3.02	0.6460	-163.42
6	0.9479	-177.28	1.0025	54.50	0.0198	4.33	0.6775	-162.98
7	0.9494	-178.19	0.8290	49.13	0.0190	6.46	0.7075	-162.94
8	0.9508	-178.96	0.6987	44.21	0.0183	9.33	0.7352	-163.19
9	0.9522	-179.65	0.5980	39.72	0.0177	12.85	0.7602	-163.63
10	0.9534	179.72	0.5182	35.61	0.0173	16.87	0.7825	-164.21
11	0.9546	179.13	0.4539	31.86	0.0171	21.23	0.8023	-164.86
12	0.9556	178.58	0.4013	28.44	0.0171	25.73	0.8198	-165.55
13	0.9565	178.06	0.3576	25.31	0.0173	30.21	0.8351	-166.25
14	0.9573	177.55	0.3210	22.46	0.0177	34.51	0.8486	-166.95
15	0.9581	177.06	0.2901	19.86	0.0183	38.53	0.8604	-167.64
16	0.9587	176.59	0.2636	17.48	0.0189	42.20	0.8709	-168.30
17	0.9593	176.13	0.2408	15.32	0.0197	45.51	0.8801	-168.95
18	0.9598	175.67	0.2210	13.35	0.0206	48.46	0.8882	-169.57

*** The data does not include gate and drain bond wires.**

SMALL SIGNAL MODEL, V_{DS} = 8 V, I_{DS} = 500 mA

SCHEMATI



PARAMETERS

Lg	0.0196 nH	**Rs**	0.197 Ohm
Rg	0.225 Ohm	**Ls**	0.005 nH
Cgs	8.87 pF	**Cds**	1.073 pF
Ri	0.455 Ohm	**Rds**	31.85 Ohm
Cgd	0.361 pF	**Rd**	0.315 Ohm
Gm	880.6 mS	**Ld**	0.004 nH
T	3.9 psec		

CHIP HANDLING

DIE ATTACHMENT: Conductive epoxy or eutectic die attach is recommended. Eutectic die attach can be accomplished with Au-Sn (80%Au-20%Sn) perform at stage temperature: 290°C ± 5°C; Handling Tool: Tweezers; Time: less than 1min.

WIRE BONDING: The recommended wire bond method is thermocompression bonding with 0.7 to 1.0 mil (0.018 to 0.025 mm) gold wire. Stage temperature: 220°C to 250°C; Bond Tip Temperature: 150°C; Bond Force: 20 to 30 gms depending on size of wire and Bond Tip Temperature.

HANDLING PRECAUTIONS: The user must operate in a clean, dry environment. Care should be exercised during handling avoid damage to the devices. Electrostatic Discharge (ESD) precautions should be observed at all stages of storage, handling, assembly, and testing. The static discharge must be less than 300V.